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Standard Gates

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Synopsis: It is shown that a three-input gate circuit, operating in accordance with switching equation $Z = pr' + q'r$, can be programmed to operate in various logical modes so that it has the character of a generally applicable standard gate. By means of feedback methods this standard gate can also be made to operate as memory element.

A number of examples is given of logic, memory and sequential circuits, that are all closely related to switching circuits commercially available as 'one-chip integrated circuits'. A price comparison shows that, also from the point of view of hardware costs, there must be a wide field of application of the standard gate circuit described in the following.

1. Introduction

The number of different digital integrated circuits is still rapidly increasing. Catalogs on integrated circuits have grown from a few data sheets to big books giving information on the many useful and effective integrated circuits now available on the market. What to choose for a specific application becomes rather difficult and time-consuming. It is even more difficult to know what to keep in stock to be able to meet a reasonable demand.

With regard to digital integrated circuits the question has been posed whether or not it will be possible to design a general-purpose gate circuit of some complexity that can be programmed to perform a number of useful different switching functions covering the whole range from simple to complex. This point cannot be settled by the simple remark that such a type of circuit will be too complex and hence too expensive for the implementation of simple logical functions. The fundamental success of integrated circuits in the digital field over circuits with lumped components is not only because of their compactness. It has also been caused by the fact that in the integrated-circuit technique more suitable circuits have been obtained with better operating features.

The prices of integrated circuits although fitted with numerous small components have reached such a low level that circuits with lumped components have become uneconomical and even obsolete in certain respects. Moreover, for integrated gate circuits no direct relation can be found between the prices of these circuits and the number of components on the chip. This leads to the question to be discussed hereafter, whether or not, at the expense of some complexity, a general-purpose gate circuit could be designed that, with all its circuitry can perform useful complex functions, and that moreover can be programmed to perform simple switching functions. The price of such a circuit can be rather low, as (because of its general applicability) it will be required in large numbers and hence has to be produced in large quantities.

Ordinary practical problems play an important role in the design of a standard gate circuit. For instance, how many terminals are required and how many terminals are available on

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the packages of integrated circuits. This is determined by the number of gates that should be combined in one package.

The scope of this discussion will be limited to Transistor-Transistor-Logic (so-called TTL) integrated circuits, produced in so-called 'dual-in-line' packages. The choice must in first instance be made between single, dual or quadruple gates in one package with 14, 16, or nowadays 18 terminals. There are also packages with 24 and more terminals but these have larger overall dimensions than the packages of the other group. The standard package (14, 16, or 18 terminals) has a width independent of the number of terminals, its length is proportional to that number.

A rational number of terminals for a package is 14, because the number of terminals of the packages of integrated circuits available for data inputs and outputs is twelve. That number can be divided by two and by four. In a dual circuit six terminals are available per circuit and in a quadruple circuit three. Hence two-wide quadruple AND, NAND, OR, NOR and exclusive-OR gates can be mounted in a 14-terminal package, but this number of terminals is not sufficient for more complex gate circuits.

If a quadruple general purpose gate circuit is to be designed, at least three inputs and one output per gate circuit are required, giving $4 \times 4 + 2$ (battery) $= 18$ terminals on the package. Until recently it would not have been possible to think of 18-terminal packages as an extension of the 14- and 16-terminal line. But this restriction has now been removed by the marketing of an integrated circuit in an 18-terminal package.

The fact that the number of two-wide quadruple gates of any kind actually sold is very large as compared with other types of gates and that wider gates can easily be designed using a number of standard gates, has been the reason why here has been chosen in favor of a *three-input quadruple standard gate*.

2. Design

The fundamental question in the design of a standard gate is, what switching equation with three input variables can best be implemented. When we consider a standard gate as an information-transfer element with one information input, one information output and two program inputs for four different modes of operation, there are only two fundamentally different types of switching equations, shown by (1) and (2): The first group represented by equation (1) consists of 8 variations and the second group represented by equation (2), showing the exclusive-OR relation, consists of 16 variations.

$$Z_1 = p'q'r + pq' + pqr' = pr' + q'r \qquad (1)$$

$$Z_2 = p'q'r + pq'r' + pq = p \oplus q'r \qquad (2)^*$$

Table 1.

p	q	Z_1
0	0	r
0	1	0
1	0	1
1	1	r'

Table 2.

p	q	Z_2
0	0	r
0	1	0
1	0	r'
1	1	1

*) The symbol $\oplus$ in this formula and elsewhere stands for the operation: 'addition modulo 2', as used e.g. in: R. M. M. Oberman: Disciplines in combinational and sequential circuit design – Mc Graw Hill Book Company, 1970.

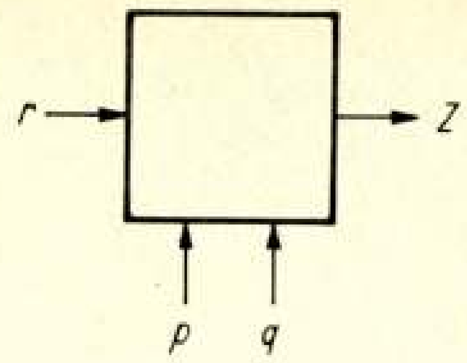


Fig. 1. 3-input gate circuit.

In Fig. 1 a block diagram is shown of this three-input gate circuit. Switching equations (1) and (2) show that a standard element operating in accordance with one of the two truth tables 1 and 2, can also function as an exclusive-OR gate. For that purpose $p = q$ in the Z_1-solution and $r = 0$ in the Z_2-solution.

It follows also from both truth tables that the two circuits operate as so-called true-complement, zero-one elements which are commercially available as special integrated circuit. Hence the implementation of a quadruple standard gate will be of about the same complexity as the already existing quadruple exclusive-OR gate or the four-bit true-complement, zero-one element, and thus will have a right of existence as standard gate independent of other features.

With two information inputs and one program wire the standard gates show the following features as given in Table 3.

Table 3.

p	q	r	Z_1	Z_2
0	–	–	$q'r$	$q'r$
1	–	–	$(qr)'$	$q + r'$
–	0	–	$p + r$	$p \oplus r$
–	1	–	pr'	p
–	–	0	p	p
–	–	1	q'	$(p \oplus q)'$

In addition to this, the switching situations with $p = q$, $q = r$, and $p = r$ must be considered. These situations are shown in Table 4.

Table 4.

	Z_1	Z_2
$p = q$	$p \oplus r$	$p + r$
$p = r$	$q'r$	pq
$q = r$	pr'	p

In the Z_1-solution the logical functions OR, NAND, exclusive-OR, PNR (*p* and not *r*), true and complement are available and in the Z_2-solution OR, AND, exclusive-OR, exclusive-NOR, PNR, true and complement can be obtained.

From the point of view of the number of different logical functions, the Z_2-solution should be preferred, however, the switching equation of the Z_1-solution shows that this type of gate circuit can easily be used as memory element. The basic circuit resulting from the Z_1-solution is very simple and effective.

The use of a standard gate in accordance with the Z_1-equation is illustrated in Table 5.

Table 5.

r	s	z	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

In this truth table Z represents the state of a set-reset trigger, controlled by input variables r and s and feedback signal z. In all cases where z and Z differ in value, the trigger will change its state in accordance with the indicated value of Z. It is noted that both trigger states with $r = s = 1$ are non-stable. Table 5 leads to the following switching equation:

$$Z = r's'z + r'sz' + r'sz + rsz' = sz' + r'z \qquad (3)$$

Switching equation (3) is identical with switching equation (1) of the standard gates.

When in the Z_1-equation (1) the variable r is clock pulse α, $p = z$ and $q = i$ (the information signal controlling the circuit), the following switching equation will be obtained:

$$Z = \alpha'z + \alpha i' \qquad (4)$$

Equation (4) is the switching equation of a so-called 'clocked latch'. The operation of this memory circuit will be explained in one of the following paragraphs.

The possible use of the standard gate Z_1 as memory element and the fact that its implementation is the simplest of the two possibilities, are the reason why this gate is chosen in this paper to be promoted as three-input standard gate. It is noted here that all possible logical operations can be obtained with this standard gate by giving it complementary outputs, but this would lead to a 22-terminal package. For the moment a 22-terminal package is still unusual and an extensive investigation in the implementation of a rather large variety of digital circuits with single-output standard gates has shown that, thanks to the PNR-function, the need for introducing extra output inverters is rather small.

3. Implementation

Drawn in ordinary gate symbols, a standard gate in accordance with switching equation $Z = pr' + q'r$ can be represented by the circuit of Fig. 2a, or by that of Fig. 2b. Because at the moment no quadruple standard gates are commercially available, their feasibility must be investigated using existing integrated circuits. The gate diagram of Fig. 2a can be implemented with e.g. SN 7402 quadruple OR gates and SN 7408 quadruple AND gates.

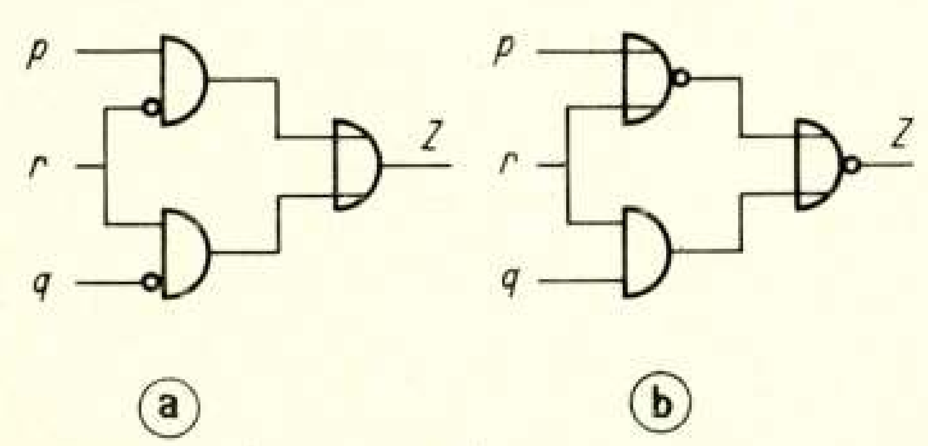


Fig. 2. Two circuits (a and b) representing a standard gate in accordance with switching equation $Z = pr' + q'r$.

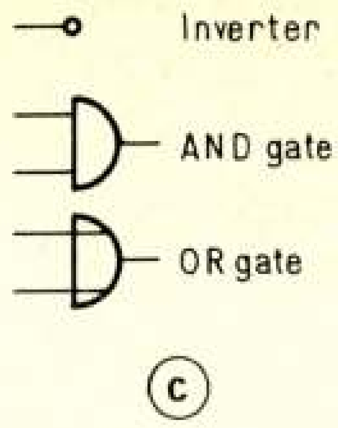


Fig. 2c. Symbols used.

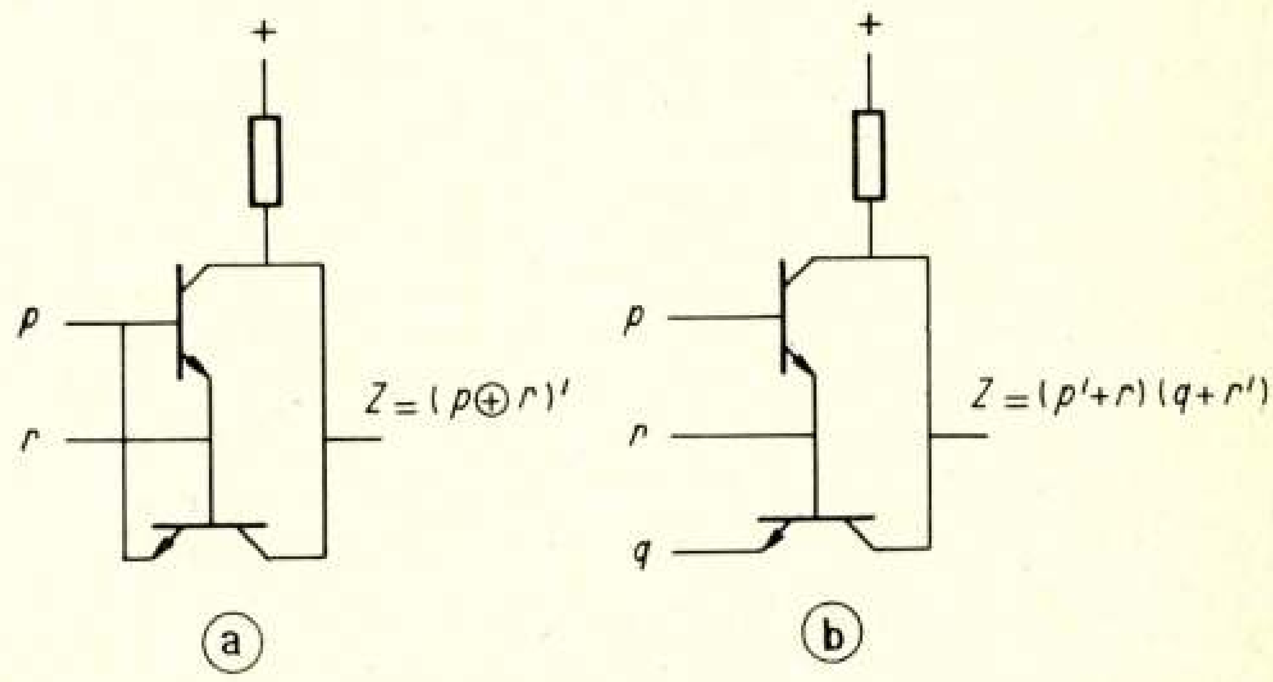


Fig. 3a. Exclusive-OR gate, operating in accordance with switching equation $Z = (p \oplus r)'$. **Fig. 3b.** Basic circuit, in which the standard gate is realized.

It is important that in the standard gate an output signal $Z = 1$ resulting from $p = 1$ and $q = 0$ is not interrupted by a reverse of input signal r from 1 to 0 or *vice versa*. It is of course possible to bridge this gap in the output $Z = 1$ by means of some extra hardware, but this complicates the standard gate slightly. In a standard gate with the following switching equation there is no gap in the output signal:

$$Z = pr' + pq' + q'r \qquad (5)$$

In switching equation (5) pq' is the bridging term, which from the logical point of view is redundant.

It has also been investigated in which way switching equation $Z = pr' + q'r$ can be implemented for integration of one chip. The catalogs of the manufacturers of integrated circuits give in their detailed circuits enough information to solve that problem. It is not necessary to have a specific knowledge of the actual integrating techniques for the design of a medium-scale digital integrated circuit. The more or less standard circuit techniques found in these detailed circuits provide enough information to find out whether or not a circuit is feasible for integration.

In the integrated exclusive-OR gates the fundamental circuit of Fig. 3a is found. In lumped components this circuit was already used in my laboratory in 1955. The switching equation is as follows:

$$Z = (p' + r)(p + r') = (p \oplus r)' \qquad (6)$$

The operation of the transistors in this integrated circuit is such that their collector-emitter path is conducting only if their base receives a control voltage in accordance with the logical 1 and

their emitter a logical 0. In all other conditions these transistors are blocking.

When splitting the interconnection between the base of one transistor and the emitter of the other transistor, the diagram of Fig. 3b is obtained that corresponds to the following switching equation:

$$Z = (p' + r)(q + r') = (pr' + q'r)' \qquad (7)$$

When the circuit cell of Fig. 3b is used as part of a larger integrated circuit, two of these cells may be used in series, without the need to provide for a means to restore the voltage level of the output signal. In the design of the standard gate, provisions must be made to enable it to be connected to the 'outside world'. Therefore input adapters must be used on the input side, and the output must be formed by a so-called 'totem-pole circuit', delivering low-impedance 0 and 1 output signals. This leads to the diagram of Fig. 4, the circuit of which operates in accordance with the following switching equation:

$$Z = [(p' + r)(q + r')]' = pr' + q'r \qquad (8)$$

This is the switching equation best suited for a three-input standard gate. There are no technical difficulties preventing the integration of this circuit as quadruple gate.

Compared with a quadruple exclusive-OR gate with the same basic diagram, 20% more transistors are involved so that its price in integrated form, because of its much greater applicability, need not be higher than that of the existing quadruple exclusive-OR gate.

In the following a standard gate will be represented by the symbol of Fig. 5. In this symbol all input adapters and output totem-poles are included. A number of rather obvious applications will now be summed up as a basis for some more sophisticated examples.

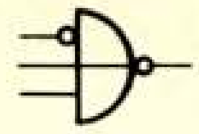


Fig. 5. Symbol for the standard gate.

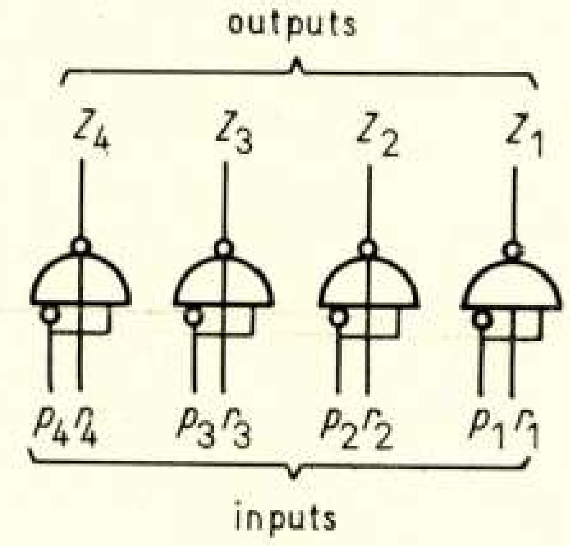


Fig. 6. Quadruple exclusive-OR gate.

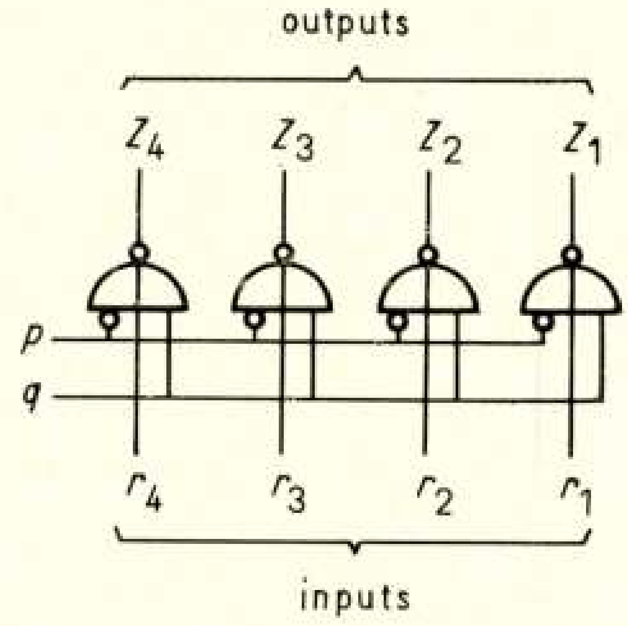


Fig. 7. 4-bit true-complement, O-1 element.

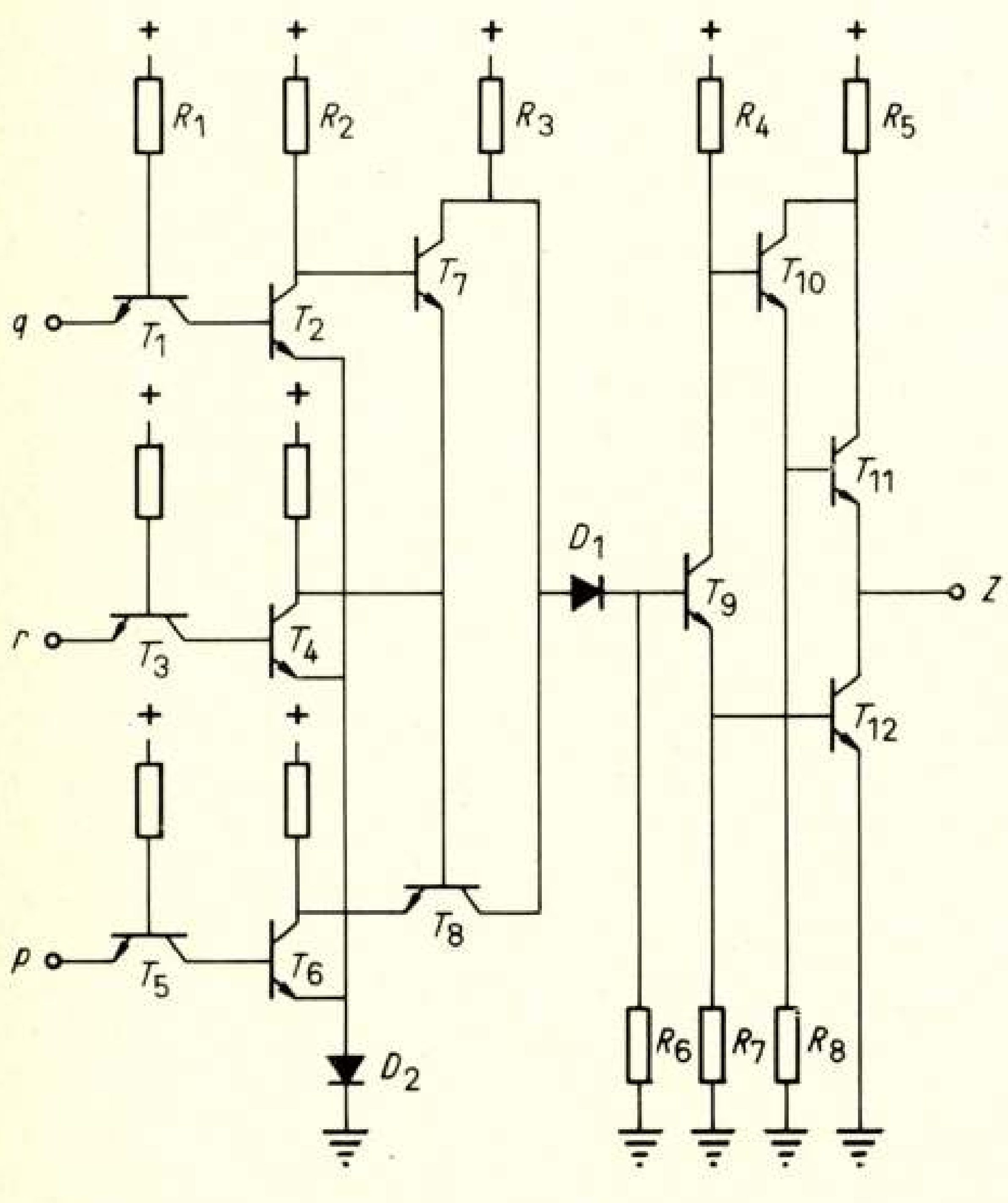


Fig. 4. Complete circuit of the standard gate.

4. Applications of the quadruple standard gate

4.1. *Quadruple Exclusive-OR Gate* (Fig. 6.)

$p = q; \quad Z = pr' \oplus p'r = p \oplus q$

In this application only 16% of the components are redundant.

4.2. 4-*Bit True-Complement, Zero-One Element* (Fig. 7.)

This element is very useful because it can connect a data line with an output in true form or in complement form, but the data line can also be blocked (0 output), or forced to generate a 1 signal. The operation of the standard gate as true-complement, zero-one element is shown in Table 6.

Table 6.

p	q	Z
0	0	r
0	1	0
1	0	1
1	1	r'

In this application six input adapters remain redundant in an element, in comparison with a similar device specially designed for this purpose.

4.3. *Quadruple Two-Wide OR Gate* (Fig. 8.)

Switching equation $Z = pr' + q'r$ reduces to $Z = p + r$ for $q = 0$. In this application 40% of the transistors are redundant when compared with a special quadruple OR gate (if existing).

4.4. *Quadruple Two-Wide NAND Gate* (Fig. 9.)

Switching equation $Z = pr' + q'r$ reduces to $Z = (qr)'$ with $p = 1$. This is the equation of a NAND gate. Compared with the specially made integrated circuit, the standard gate shows a redundancy of about 60%.

4.5. *Quadruple PNR Gate* (Fig. 10.)

The basic switching equation of the standard gate reduces to

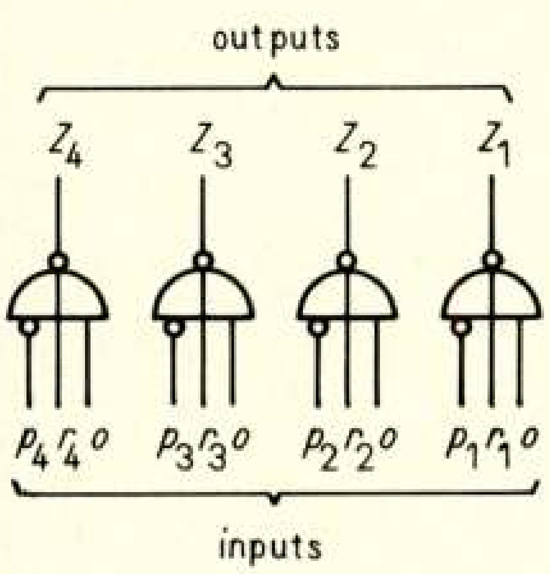


Fig. 8. Quadruple 2-wide OR gate.

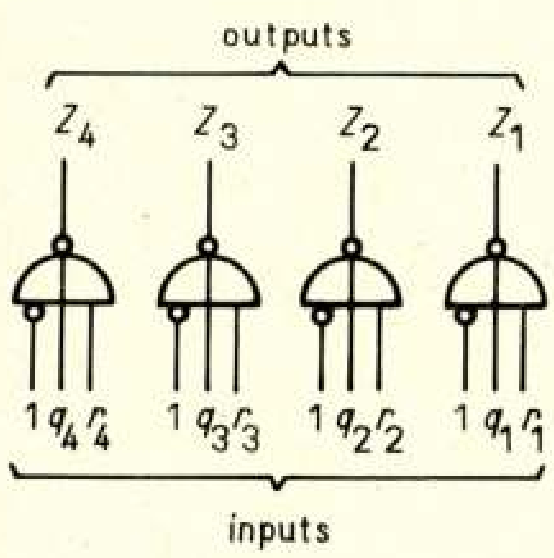


Fig. 9. Quadruple 2-wide NAND gate.

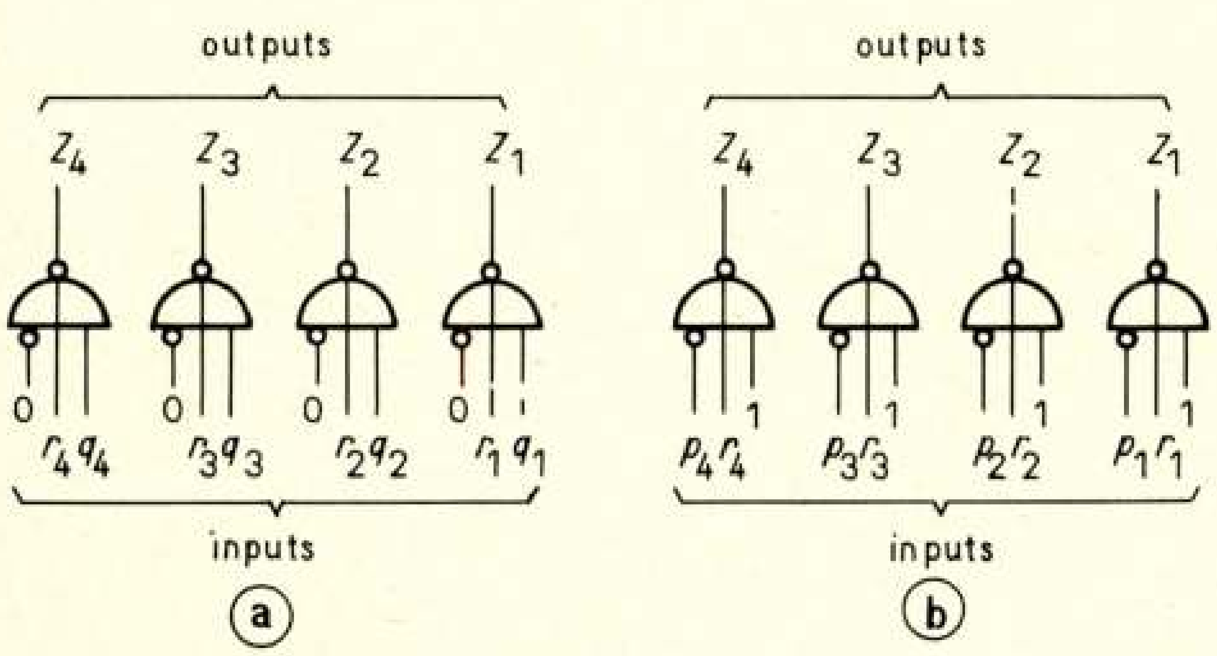


Fig. 10. Quadruple PNR gates.

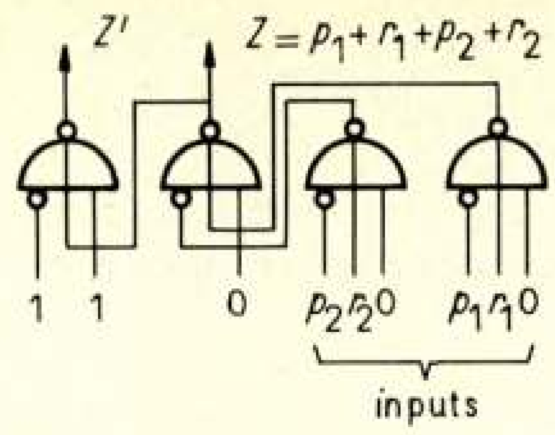


Fig. 11. 4-wide OR gate.

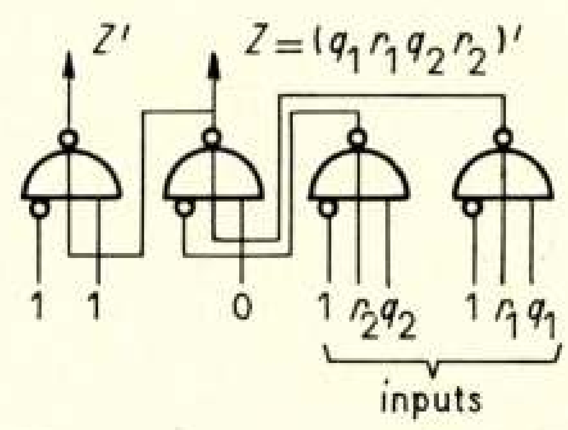


Fig. 12. 4-wide NAND gate.

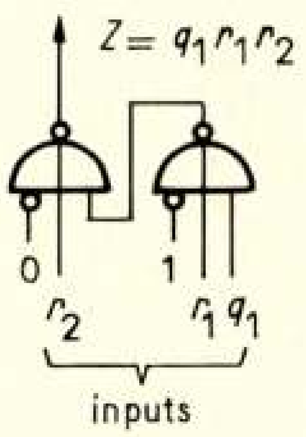


Fig. 13. 3-wide AND gate.

$Z = q'r$ with program signal $p = 0$ or to $Z = pr'$ with program signal $q = 1$. These possibilities are shown in Figs. 10a and 10b respectively.

This function is very useful because in many cases its application makes it unnecessary that complemented variables should be generated by the memory elements of the circuit, or that they should be generated by the insertion of extra inverters.

4.6. *Four-Wide OR Gate* (Fig. 11.)

A four-wide OR gate can be obtained by combining a number of standard gates, as is shown in Fig. 11. Two two-wide OR gates combine to make a four-wide OR gate by means of a third two-wide OR gate. This procedure can be extended as long as the signal propagation delay along the complete circuit does not become prohibitively high. For each doubling of the number of inputs one gate delay time has to be added.

A four-wide NOR gate is obtained by adding an inverter to the four-wide OR gate, as is also shown in Fig. 11.

4.7. *Four-Wide NAND Gate* (Fig. 12.)

With program signal $p = 1$ the basic switching equation becomes as follows:

$Z = r' + q'r = (qr)'$

The outputs of two of these gates combined by an OR gate give

a four-wide NAND gate as follows from its switching equation:

$$Z = (q_1' + r_1') + (q_2' + r_2') = (q_1 q_2 r_1 r_2)'$$

With an extra standard gate programmed as inverter, a four-wide AND gate is obtained. Seven standard gates are required to form an eight-wide NAND gate.

4.8. *Three-Wide AND Gate* (Fig. 13.)

In the first standard gate $(q_1 r_1)'$ is formed (NAND gate) and in a second standard gate programmed for PNR-operation the following switching function will be obtained:

$$Z = [(q_1 r_1)']' r_2 = q_1 r_1 r_2$$

5. Standard gates used as memory elements

5.1. *Clocked latch*

This circuit (Fig. 14.) operates in accordance with the following state equation:

$$Z = pr' + q'r = \alpha' z + \alpha i' \qquad (9)$$

$Z = z$ during clock pulse phase $\alpha = 0$. This is the memory function. $Z = i'$ during clock pulse phase $\alpha = 1$. In this phase of the clock pulse the memory element can be set by a new information signal, but the complement of that signal is stored. Especially when a PNR gate is available, the complemented storage of information will not be a disadvantage of this type of single output memory element.

5.2. *D-type master-slave memory element*

With two clocked latches a D-type MS memory element as shown in Fig. 15 can be formed. The master part of this memory element operates on an α clock pulse, then the slave part must operate on an α' clock pulse so that $\alpha\alpha' = 0$. Otherwise a short circuit between information input i and information output Z can arise, possibly leading to an erroneous circuit operation. The series connection of both complementing latches results in the following switching equation:

$$Z = D_\alpha(i) \qquad (10)$$

This equation states that under the control of clock pulse α the next state of Z will have the logical value of i.

It is noted that the D-type flip-flop is in fact a shift register section.

By connecting standard gates to the input of a D MS flip-flop, other types of flip-flops can be realized. There are only two fundamentally different types of two-input MS flip-flops, in the same way as there are only two fundamentally different types of three-variable gates.

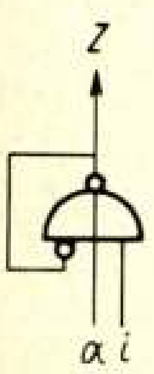


Fig. 14. Clocked latch.

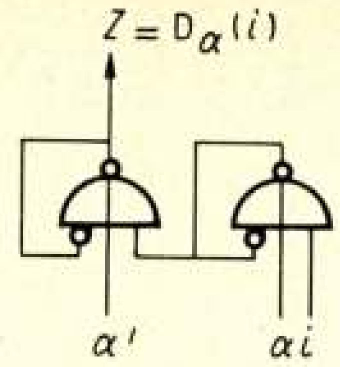


Fig. 15. D-type master-slave flip-flop.

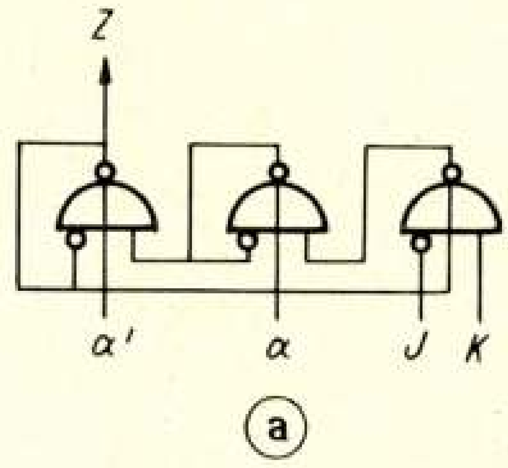


Fig. 16a. JK flip-flop.

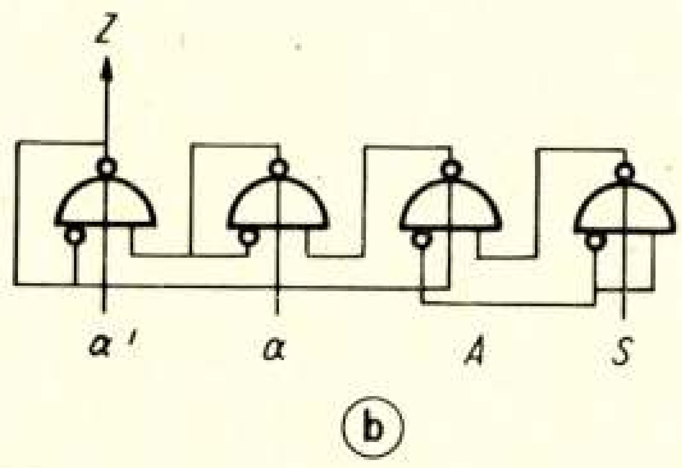


Fig. 16b. AS flip-flop.

Under control of two external inputs and one feedback input, only 0, 1, z, and z' can be obtained as output. In relation to the two input signals these four possible output signals can be arranged in 24 different ways. These 24 ways can be split up into two fundamentally different groups, to be called the JK and the AS group. Truth Tables 7 and 8 show a suitable representative of each group.

Table 7.

J	K	Z_{n+1}
0	0	z_n
0	1	0
1	0	1
1	1	z_n'

Table 8.

A	S	Z_{n+1}
0	0	z_n
0	1	0
1	0	z_n'
1	1	1

The arrangement of truth Table 7 leads to the following switching equation:

$$Z_{n+1} = D_\alpha(J'K'z_n + JK' + JKz_n') = D_\alpha(Jz_n' + K'z_n) \qquad (11)$$

This is the switching equation of the well-known JK master-slave flip-flop. This equation can be implemented with three standard gates. The circuit is in fact a D master-slave flip-flop

preceded by one standard gate which changes its D type features in JK features. The resulting circuit is shown in Fig. 16a.

The right-hand truth table (Table 8) corresponds to the following switching equation:

$$Z_{n+1} = D_\alpha(A'S'z_n + AS'z_n' + AS) = D_\alpha[Az_n' + (A \oplus S)'z_n] \quad (12)$$

This shows that with $A \oplus S = K$ or $A' \oplus S' = K$, and $A = J$ the AS flip-flop can be obtained from the JK flip-flop by means of an extra exclusive-OR gate connected to its K input. A number of variations is possible. The diagram of this flip-flop is shown in Fig. 16b.

The more complicated AS flip-flop has the advantage that its operation can easily be changed from that of a shift section into that of a pulse halver or binary counter section, under control of the S' signal.

6. Application of memory elements

In the foregoing a number of gate circuits and memory elements have been composed by means of a standard gate circuit. Theoretically this opens the possibility of implementing all digital circuits using one building stone, the standard gate, and nothing else. This proposition is in certain respects of the same quality as the fact that all digital circuits can be implemented using transistors only. Both possibilities of implementation have their limitations which depend on the features of the more complicated circuits in which their application is still practical. In another paper dealing with the 'Standard Accumulator' it will be shown that there is at least place for one more such a complicated circuit.

In the following some more applications of the standard gate that may be possible will be given and discussed. Additional examples of the general applicability of the standard gate will be found in the paper on the 'Standard Accumulator', just mentioned.

6.1. *Odd-even parity generator/checker*

With this type of circuit a parity check bit can be generated in addition to a word or number at the input, or the parity can be checked of a received input word or number containing a parity bit. In the diagram of Fig. 17 an eight-bit (expandable) diagram is shown, having eight data inputs 1 ... 8 inclusive and a ninth input, marked 0.

When using the circuit for checking a received number, the number has to be fed to the normal inputs and the received parity bit to the control input 0. The resulting output signal of the circuit will remain in the same logical state until an odd number of bits is lost during transmission. The given diagram is that of a circuit being equivalent to the NS DM 7220/DM 8220 8-bit parity checker/generator and also equivalent to the slightly different SN 54180/SN 74180 8-bit circuit.

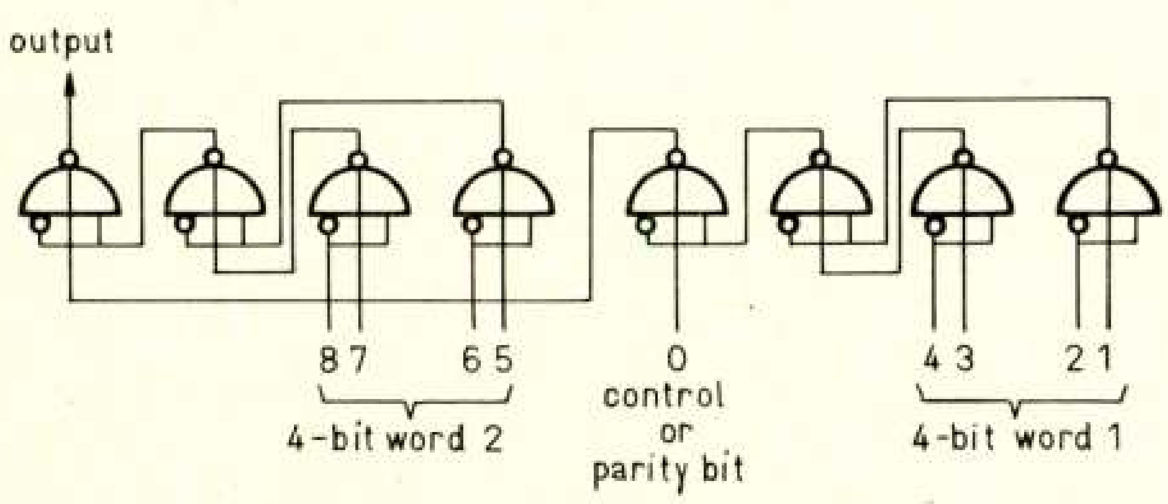


Fig. 17. Odd-even parity generator/checker.

The fact that two quadruple standard gates are required for an eight-bit parity checker/generator and the fact that such a circuit is commercially available in one package, do not disqualify the quadruple standard gate for use as parity checker.

If the price of the quadruple standard gate is the same as that of a quadruple two-input exclusive-OR gate, then the comparable price of the eight-bit odd-even parity checker/generator is $1\frac{1}{6}$ times higher than that of two quadruple standard gates. If, and that can readily happen, the one-chip eight-bit odd-even parity checker/generator has to be purchased in small numbers this ratio can increase to about 1.9. If in excess of that the one-chip circuit has to be ordered separately, the price will increase once more invisibly many times. Even with a more unfavorable price the quadruple standard gate will be practicable for this application. In many other applications the same price trend will be encountered.

6.2. *Four-bit magnitude comparator*

A four-bit magnitude comparator is commercially available in one dual-in-line package. This circuit compares the magnitude of two four-bit binary numbers in terms of $A > B$, $A = B$, $A < B$. Notwithstanding the fact that this circuit shows parallel operation, its operating time consists of five gate delays.

Using the standard gate as building stone, an elegant circuit on serial basis can be designed having the same operating time and having the same cascading features as the commercially available magnitude comparator. The diagram of Fig. 18 shows a four-bit circuit in this arrangement.

In fact $A > B$ and $A < B$ are determined. From the result $A > B$ and $A < B$, $A = B$ can be concluded unambiguously. This feature can be considered as an *extra* which need not be part of *all* four-bit comparators, but which can be added to the last four-bit portion of a comparator for words of N bits.

In the magnitude comparator of Fig. 18 use is made of the standard gate as true-complement, zero-one element for the eight standard gates appearing in the horizontal central lines. The extra gates in the individual input lines, generating functions ab' and $a'b$ are required to suppress the complementing feature of the central line gates. These extra gates generate a logical 1 only when $A > B$ or $A < B$, so that the central line gates never are fed with two 'ones' simultaneously. A central line gate fed with two 'zeros' transmits the logical value on its central input to the next gate ($A = B$). A central line gate receiving a 1 from its corresponding input gate and hence a 0 from the corresponding input gate on the other side of the central line, transmits a 1 to the next stage of the comparator. The corresponding gate in the other central line is then blocked so that no 1 signal from lower order stages can be transmitted to higher order stages.

Larger numbers can be compared, using the $A > B$ and $A < B$ inputs for the results of the comparison of higher order bit groups in these numbers. Because all digits a_4 ... a_7 and b_4 ... b_7 have a weight greater than that of a_3 and b_3, the result of comparing bit groups a_4 ... a_7 and b_4 ... b_7 can be injected in the central lines, as is shown in Fig. 18. The time thus required for comparison increases with one gate delay for every four bits added.

The price of the one-package four-bit magnitude comparator is about 0.85 of that of the four quadruple standard gates used in this example and that ratio increases to about 1.4 when only

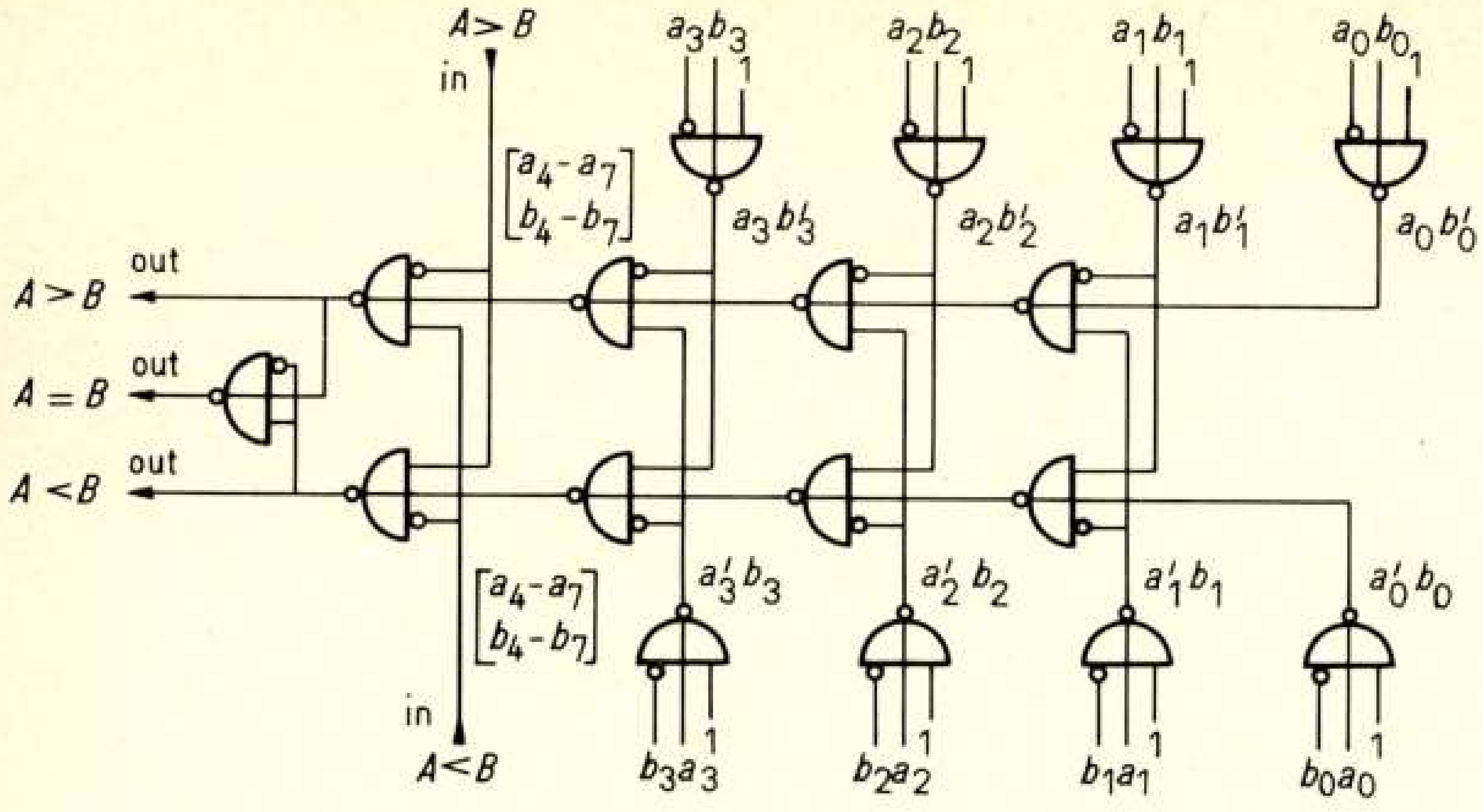


Fig. 18. 4-bit magnitude comparator.

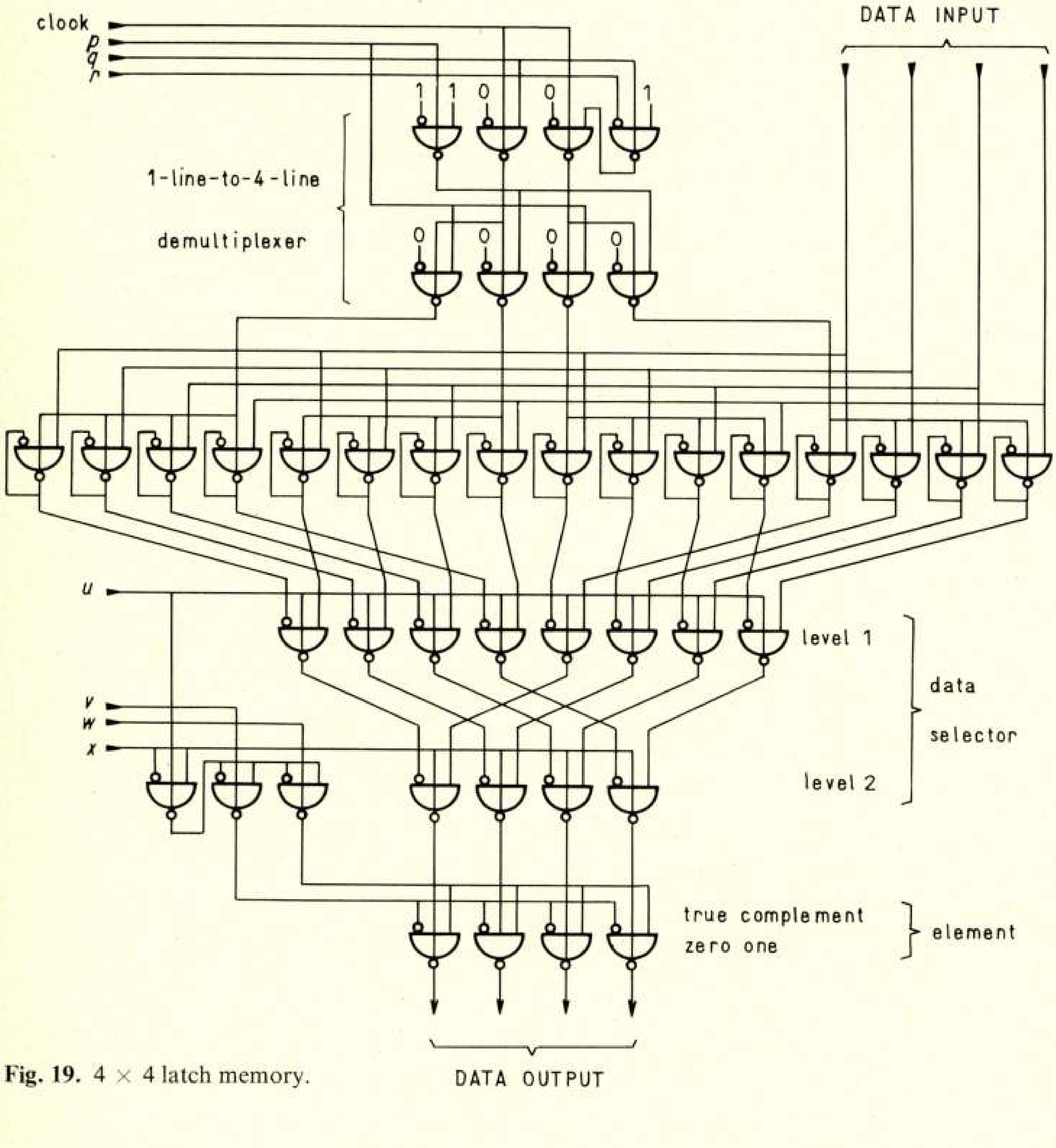


Fig. 19. 4 × 4 latch memory.

small numbers of the single four-bit magnitude comparator are required. It is noted here that in our example some extra costs must be taken into account if the $A = B$ feature is required, as well including the costs resulting from extra space and mounting.

6.3. *A* 4 × 4 *latch memory*

A 4 × 4 latch memory can easily be designed using standard gates for the 16 memory elements (D-type latches) and for the 1-line-to-four-line demultiplexer to direct the clock pulse to the

group of latches to be operated. When using the standard gate as latch memory element, the output data are presented in complemented form with respect to the input data. This will cause no trouble when the memory is used in co-operation with the 4 × 4-line-to-1-line Data Selector/Multiplexer to be described hereafter, because in the Data Selector/Multiplexer all data can be complemented.

In the top of Fig. 19 the diagram of the actual 4 × 4 latch memory is shown, in the bottom of this figure the diagram is shown of the data selector to be described in the next paragraph.

The data input lines (words of four bits) of the 4 × 4 latch memory are multipled over the four groups of four input lines of the word memories. Which of the groups of latches is operated by the incoming data is determined by program wires p and q of the 1-line-to-4-line demultiplexer consisting of two quadruple standard gates. Signals p and q determine the position of the demultiplexer, i.e. to which group of latches the operating clock pulse is directed. Signal r (together with q) can block the operation of the circuit.

6.4. *A* 4 × 4-*line-to-*1-*line data selector-multiplexer*

In many applications the 4 × 4 latch memory has to be supplemented for further use with a 4 × 4-line-to-1-line data selector/multiplexer. When using the standard gate as a 2-line-to-1-line selector, the data on one input will pass through this switch in their 'true' form and the data via the other input will appear at the output in 'complemented' form. This complementing can be neutralized by adding a standard gate in the output circuit which is programmed as true-complement, zero-one element. By cascading two levels of standard gates, 4-line-to-1-line data selectors/multiplexers can be formed. The diagram of Fig. 19 shows a quadruple 4-line-to-1-line data selector, followed by an extra quadruple true-complement, zero-one element for the control of the true-complement form of the output data signals.

The four data selector positions are controlled by program signals u and x. Table 9 shows in what form the output data signals of switch level 2 will appear as a function of the selector position signals u and x.

Table 9.

u	x	Signal mode level 2	v	w	Signal mode data output
0	0	complement	1	1	true
0	1	true	1	1	true
1	0	true	1	1	true
1	1	complement	1	1	true

The $u \oplus x$ supervising signal controls the v and w programme signals in such a way that in all positions of the data selector the data signals pass either in true or in complement form, as may follow from Table 9. With program signals $v = w = 0$, the signal mode of the output data will be 'complement' in all data selector positions. In addition to these features, the data transport through the data selector can be blocked or be replaced by 1-signals.

In the diagram of Fig. 19 five quadruple standard gates are required for the data selector. Comparison of the price of this circuit with its equivalent in special-purpose integrated circuits is not so easy because in our example an extra true-complement, zero-one element is required in order to obtain the same fase for all groups of data output signals. There is no need for this when using a special-purpose 4-line-to-1-line data selector. However, the true-complement, zero-one element used in the output of Fig. 19 gives some useful extra features which could also be required when using special-purpose integrated circuits instead of standard gates. In that case the circuit built with standard gates shows an important economic advantage over that designed with special-purpose integrated circuits. The hardware price ratio is 1.4 in the advantage of the standard gate solution, which ratio may increase to 2.3 depending on the required number of special-purpose integrated circuits.

6.5. *Quadruple bistable latch*

It is noted here that one quadruple standard gate can also be used as quadruple bistable latch. In the example of the 4 × 4 latch memory use is already made of this feature, but no price comparison was made between both competing packages. In certain respects this is difficult because the special quadruple latch has a true and a complement output, whereas the standard gate latch has one output only. On the other hand the special-purpose commercially available dual quadruple bistable latch has also one output only, which makes it more reasonable to compare the actual prices. The price ratio between a quadruple bistable latch and a quadruple standard gate is 1.5, increasing to 2.5 when small numbers of the quadruple bistable latch have to be purchased. The price ratio between a dual quadruple bistable latch and two quadruple standard gates (also giving eight single output bistable latches) is even more in favor of the standard gate solution. This ratio is 1.8, increasing to 3.1 when small numbers of the special-purpose dual quadruple bistable latch have to be purchased.

6.6. *Shift registers*

The discussion of examples showing applications of the standard gate may be continued by paying attention to the design of a few shift register and counter circuits. These designs do not have the pretention of being economical compared with the special integrated circuits for the same purpose, and moreover they will generally require more space. These circuits are given for completeness sake, to show that the applicability of the standard gate is not limited to combinatorical logical and to memory circuits as discussed in the preceding paragraphs.

A four-bit shift register (Fig. 20) can readily be designed with D-type MS flip-flops. The most desirable features of a shift register are given in Table 10. A shift mode of operation is, of course, necessary and the features of parallel load and reset-to-zero ('clear') are highly desirable.

Table 10.

p	q	Mode
0	–	shift
1	0	clear
1	1	load

For this purpose two standards gates (SG_{1-2}) are used between successive D flip-flops. Standard gate SG_1 of each section, used as a two-position selector, is controlled by program signal p. The shift information s_i is fed to its top terminal, and its bottom terminal is connected with the output of standard gate SG_2. In each section of the shift register standard gate SG_2 is con-

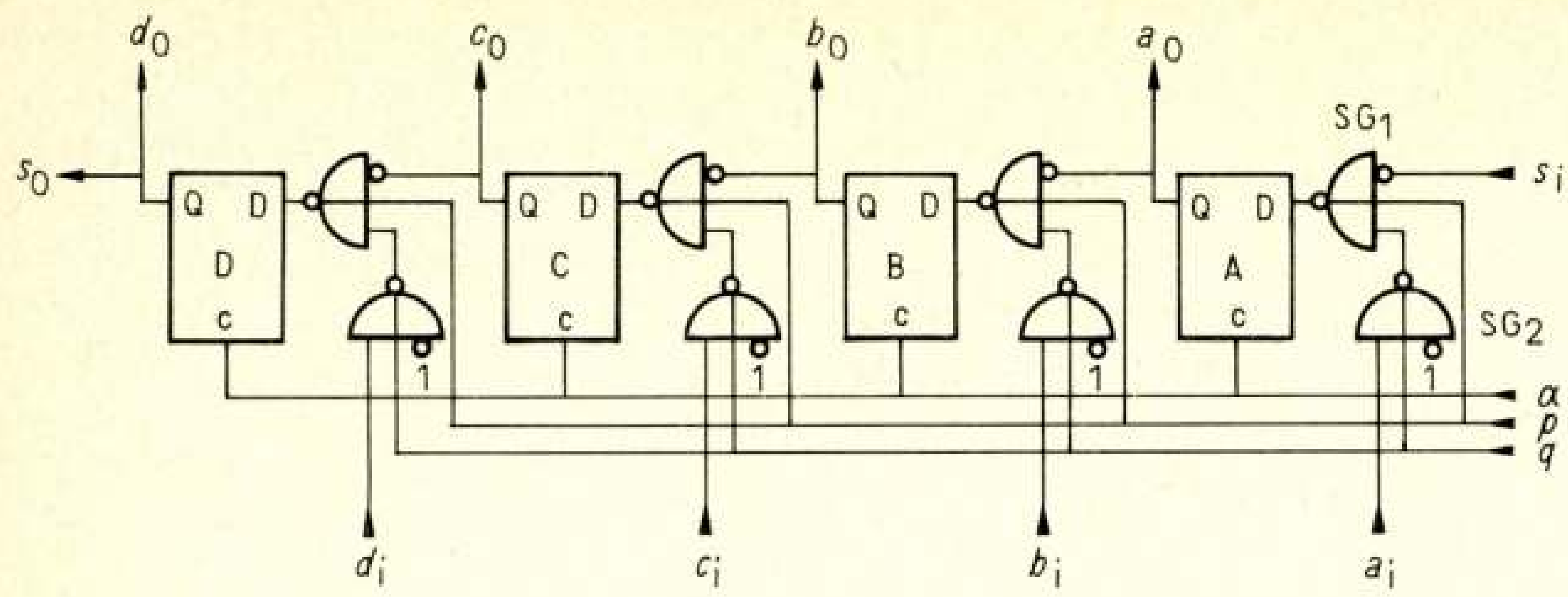


Fig. 20. 4-bit shift register.

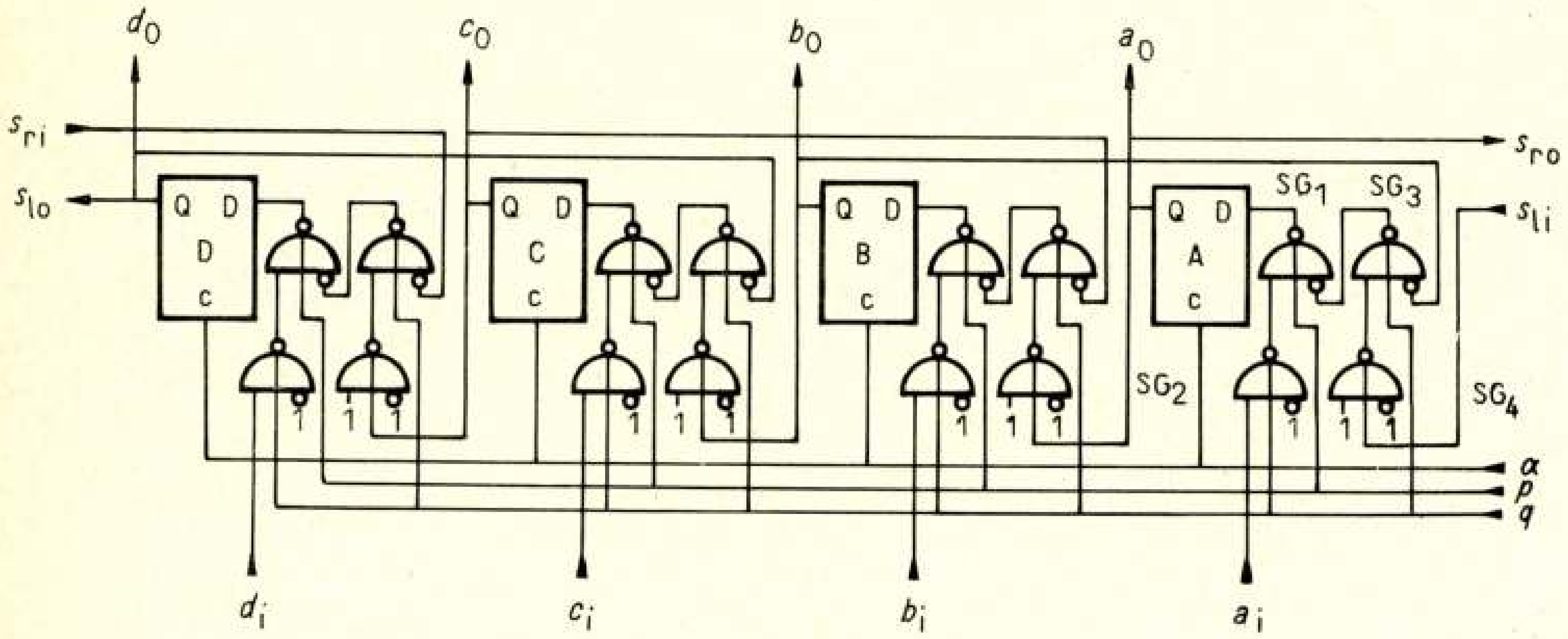


Fig. 21. Left-shift, right-shift register.

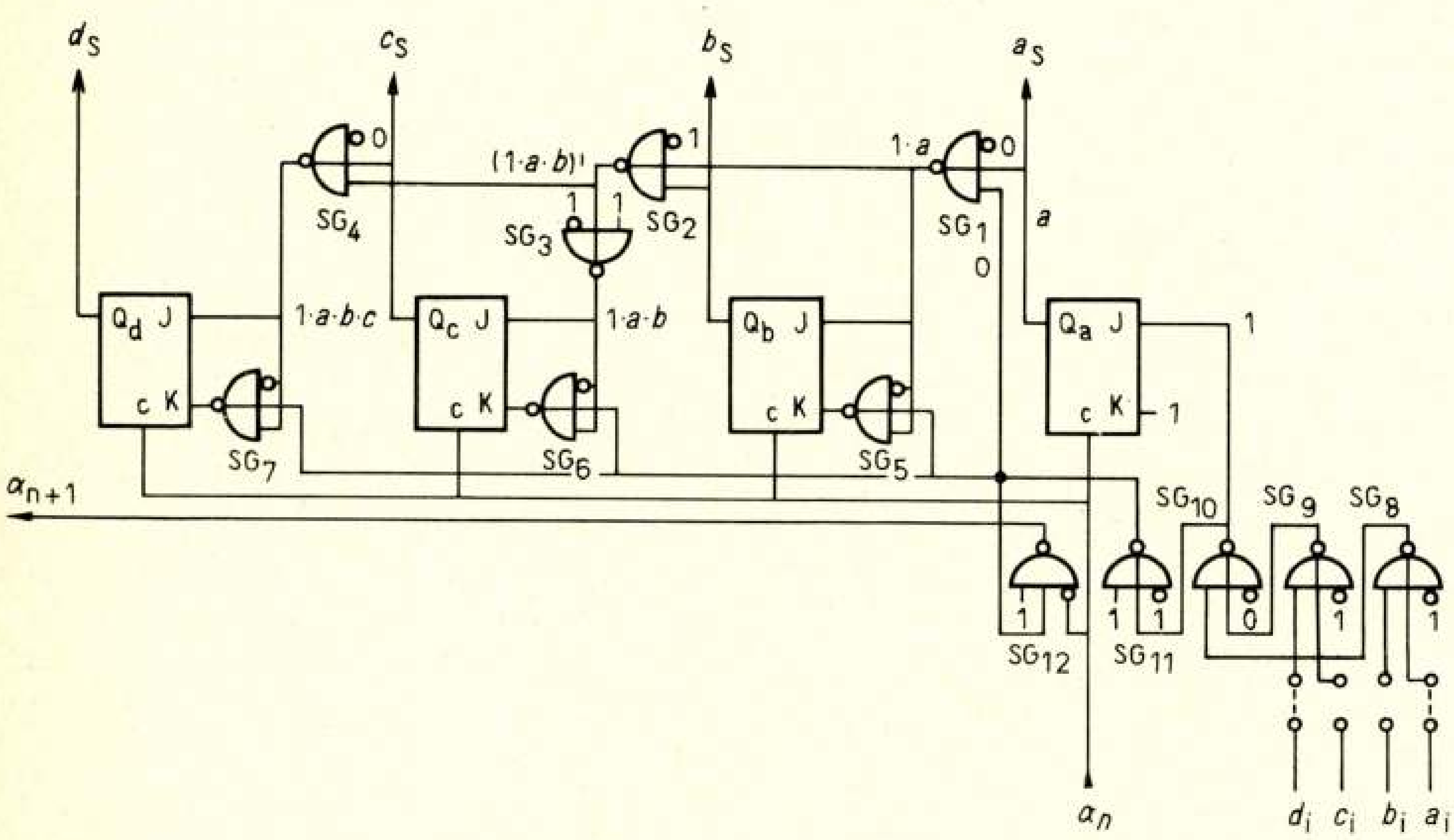


Fig. 22. 4-section synchronous binary-coded divide-by-N counter.

trolled by program signal q. The right hand terminals of all gates SG_2 are controlled by a 1-signal. If $q = 0$, the 1-signal, after being complemented by gate SG_1, is fed as a 0 to the D flip-flop of a section. This results in a general reset to 0 ('clear') of all sections. At $q = 1$ preset inputs a_i, b_i, c_i, d_i are connected with the corresponding flip-flop so that the shift register can be loaded in parallel.

In Fig. 20 the D flip-flops are shown as rectangles and not as a standard gate circuit. This emphasizes the fact that the standard gates can also be used in connection with other types of integrated circuits.

The shift register of Fig. 20 can easily be extended to a left-shift, right-shift register, the diagram of which is shown in Fig. 21. In that diagram standard gates SG_{1-2} have the same func-

tion as the standard gates SG_{1-2} in Fig. 20. The left-shift and right-shift information is fed to gate SG_1 via standard gates SG_3 and SG_4 under control of program signal q. With $q = 0$ the output of a higher order section of the shift register is connected to the input of the next lower order section, so that right-shift is obtained. With $q = 1$ left-shift is obtained. Standard gate SG_4 in the left-shift interconnection path is programmed as inverter to compensate for the complementing of SG_3, programmed with $q = 1$. The operation of this shift register is summarized in Table 11.

Table 11.

p	q	Mode
0	0	shift →
0	1	shift ←
1	0	clear
1	1	load

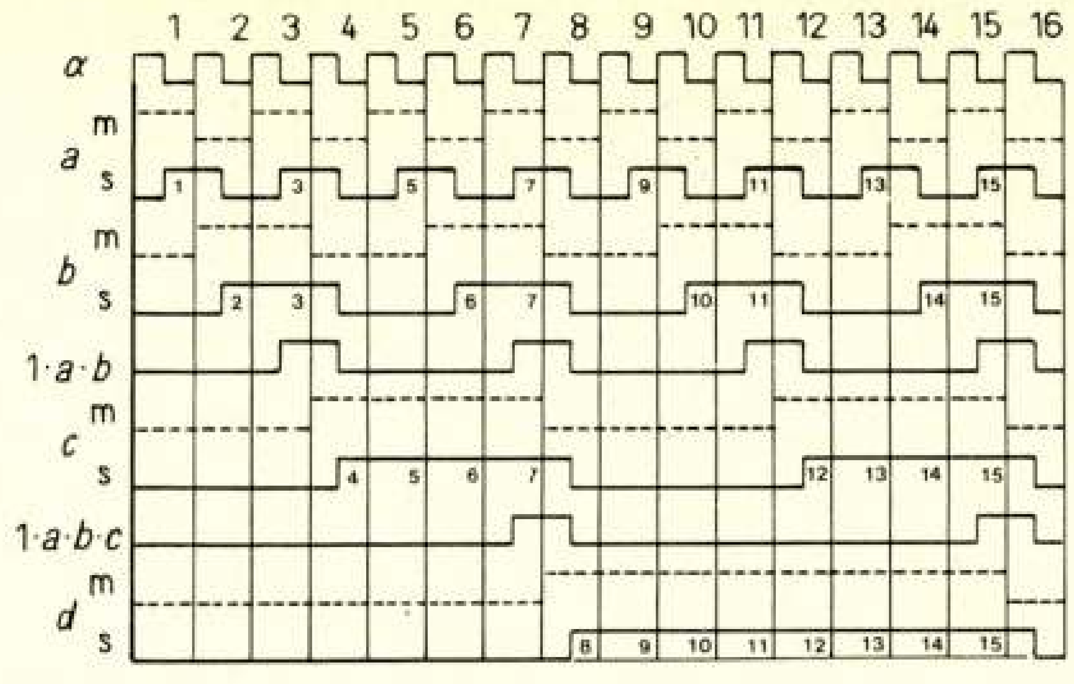


Fig. 23. Time chart showing the counting cycle of the binary-coded divide-by-N counter of Fig. 22.

The shift register of Fig. 21 is provided with left-shift and right-shift input and output terminals (s_{li}, s_{lo}, s_{ri}, s_{ro}) so that it can be cascaded.

Both shift register circuits have parallel input, parallel output, serial input and serial output so that all kinds of shift operation can be performed.

6.7. *Synchronous binary coded divide-by-N counter (BCDN)*

As a final item the design of an up-counting synchronous binary coded divide-by-N counter will be discussed. A four-section circuit of such a counter is shown in Fig. 22, the corresponding time chart in Fig. 23. In this diagram use is made of JK flip-flops as memory elements. These flip-flops are indicated as blocks in order to show that the synchronous counter arrangement given in Fig. 22 is of a general nature. The logical part of the circuit giving the synchronous counting operation of the JK flip-flops, however, is shown in standard gates.

The time chart of Fig. 23 shows on the lines a, b, c, and d the operation of the four JK flip-flops involved. Lines m show the operation of the master or input part of a flip-flop, lines s show the operation of the slave or output part of a flip-flop.

A JK flip-flop operates as a pulse halver with $J = K = 1$. This operation is blocked at $J = K = 0$. Each K input (except that in the first section) is connected with the output of an exclusive-OR gate ($SG_{5...7}$). During the counting operation the output of standard gate SG_{11} marks one input of the gates $SG_{5...7}$ with 0 so that in all JK flip-flops the J and K inputs receive the same control signals. This means that the J input and the corresponding input of the exclusive-OR gate of each section (except the first section) can be controlled by a single wire. If the signal state on this wire is 0, the binary operation of the JK flip-flop is blocked for all further counting pulses α; if this signal state is 1, the JK flip-flop will reverse its state on each counting pulse α received during that signal state.

It is shown in the time chart of Fig. 23 that the JK_b flip-flop operates synchronously when the JK control signal is a, that the JK_c flip-flop operates synchronously when the JK control signal is $1 \cdot a \cdot b$, etc. Standard gates $SG_{1...4}$ provide these control signals.

All the JK control signals become simultaneously 0 when the output of SG_{11} changes from 0 to 1. This change in output of SG_{11} makes, via standard gates $SG_{5...7}$, the J and K input signals of flip-flops $JK_{b...d}$ differ, so that all J become 0 and all K become 1.

Because output SG_{10} changes from 1 to 0 when output SG_{11} changes from 0 to 1, all JK flip-flops of the counter will be reset to 0 on the next counting pulse α.

The reset to 0 of the counter of Fig. 22 is controlled by a plug board. The two dotted lines show the connections to be made for a decade counter. On the ninth counting pulse α ($dcba = 1001$) gates $SG_{8...10}$, co-operating as a four-wide NAND gate, produce a 0 signal which is complemented by gate SG_{11} into a 1 signal. On the tenth pulse of each counting cycle, these signals change the operating conditions of the counter into reset conditions so that the next counting cycle will be started from the all-zero state of the counter. Any of the numbers 1 ... 15 can be preset in the plugboard.

By means of gate SG_{12} counting pulse α_{n+1} for the next decade or group of sections can be generated in a synchronous mode. It is noted that all sections of this counter operate in a completely simultaneous mode on α counting pulses. There is no gradual delay of this pulse in operating the successive sections of the counter.

6.8. *Half adders and Full adders*

For the sake of completeness it is mentioned here that with two standard gates five different half adders can be designed. With three or four standard gates 16 full adders are possible, all having one standard gate only for 'carry' generation.

7. Conclusion

It follows from the preceding that a standard gate operating in accordance with switching equation $Z = pr' + q'r$ has a wide field of practical and economical application in digital switching, not only in logical circuits but also in some types of memory and sequential circuits.

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'Large-Scale Integration' in MOS-technieken

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Synopsis: *Large-Scale Integration in MOS-technique.*
In the design of electronic desk calculators the MOS-technique has led to a completely new concept, in which 'data routers' and 'read-only memories' play an important role. Thanks to the automated development of these circuits a very flexible approach has been reached, while still achieving a high degree of integration.

Masks are now prepared by means of a photographic mask generator and a computerprogram called CIRCUITMASK. This method saves labour in development and avoids errors, especially in the MOS-technique, where identical subcircuits are likely to be repeated many times to form the whole circuit.

1. Inleiding

De metaal-oxyde – halfgeleider-techniek met haar schakelingen van kleine afmetingen en lage dissipatie is bijzonder geschikt voor 'large-scale integration'. Deze techniek stelt ons voor twee vragen:

a. Wat zetten wij op één kristal?
b. Hoe zetten wij dit erop?

Als voorbeeld van een uitvoering in 'large-scale integration' zullen wij enkele schakelingen bezien uit een serie, die als 'FE-reeks' zal worden geannonceerd. Deze schakelingen zijn in de eerste plaats ontwikkeld voor een tafelrekenmachine. In verband met de voor deze ontwikkeling beschikbare tijd waren er enkele praktische beperkingen. Als fabricageproces moest een zgn. *hoge spannings p-kanaal proces* worden gebruikt; de voedingsspanning is -27V; als omhulling was alleen een 16-pens omhulling beschikbaar.

Voor de schakelingen werden statische schakelingen gekozen omdat deze zonder bezwaar op de bestaande automatische meetapparatuur getest konden worden, voorts omdat het ontwerp minder risico gaf en omdat de 'timing' in de schakelingen zowel als in de rekenmachine in zijn geheel geen problemen gaf.

Door deze beperkingen zijn de schakelingen niet bijzonder geavanceerd, doch zij kwamen wel op tijd klaar. Zij blijken met een goede opbrengst te produceren te zijn. Omdat wij het aantal informatiewegen en daarmee het aantal pennen minimaal hebben willen houden werd voor een uitvoering als serie-machine gekozen. De machine werkt met 16 decimale cijfers; van ieder cijfer staan de 4 bits eveneens in serie, zodat de schuifregisters 64 bits lang zijn. Om het resultaat van de berekeningen voldoende snel beschikbaar te hebben was een klokfrequentie van ongeveer 250 kHz nodig, die gemakkelijk kon worden bereikt.

2. Wat op één kristal?

De vraag is nu: Wat zetten wij op één kristal? Een voor de hand liggende methode is, op de gebruikelijke manier een ontwerp te maken en dit dan in een aantal stukken te delen. Men ervaart dan, dat bepaalde stukken een regelmatige structuur hebben (registers bijv.) terwijl andere stukken zgn. *wilde logica* bevatten.

Om deze wilde logica te maken zou men zgn. 'gate arrays' kunnen ontwerpen. Men staat dan echter voor enkele problemen, nl. hoe moet men het verbindingspatroon tussen de poorten ontwerpen en hoe de testprocedure. Zo'n 'gate array' past ook niet erg in de MOS-techniek. De verbindingen vergen veel plaats, zeker driekwart van het kristal.

Vroeger kostten de poorten het meeste geld. Men moest hun aantal dus minimaliseren, terwijl de verbindingen in de gedrukte bedrading op de kaarten lagen en geen extra geld kostten.

In de MOS-techniek liggen deze dingen anders: de verbindingen kosten meer ruimte dan de onderdelen. Men moet *daar* naar *regelmatige* structuren streven.

3. Nieuwe opzet van machine

3.1. *Functionele aanpak*

In ons Applicatielaboratorium, het C.A.B., waar men reeds jaren aan tafelrekenmachines heeft gewerkt, werd een nieuwe opzet van de machine uitgewerkt, waarbij de zaak functioneel werd aangepakt. Iedere rekenmachine bevat een aantal delen: het ingangsdeel, het geheugendeel, het rekenkundig gedeelte, het uitgangsdeel en het besturingsgedeelte (fig. 1a). Het besturingsgedeelte vormt daarbij de wegen welke de signalen voor de gewenste bewerkingen moeten volgen. Voor dit besturingsgedeelte heeft men een nieuwe, functionele aanpak gevonden, zoals in fig. 1b weergegeven.

Tussen de onderdelen van de machine bevinden zich als schakelingen 'data routers', ook wel *multiplexers* genaamd. Door middel van 4 adresingangen kan men uit 16 verschillende combinaties van verbindingen tussen ingangen en uitgangen een keuze maken, die bepaalt welke van de verschillende voorkomende bewerkingen verricht moet worden. De adresingangen worden bestuurd door een 'read-only memory', een vast geheugen dat de microprogramma's bevat. De 'data router' en het 'read-only memory', welke sterk op elkaar lijken, zijn zeer regelmatige structuren, met aluminiumlijnen en diffusiebanen loodrecht op elkaar, wat zeer voordelig is. In fig. 2 is hiervan een voorbeeld afgedrukt.

Voordracht, gehouden tijdens de 213e werkvergadering van het NERG, op donderdag 17 december 1970 in het gebouw van de Afdeling der Elektrotechniek van de T.H. Delft.

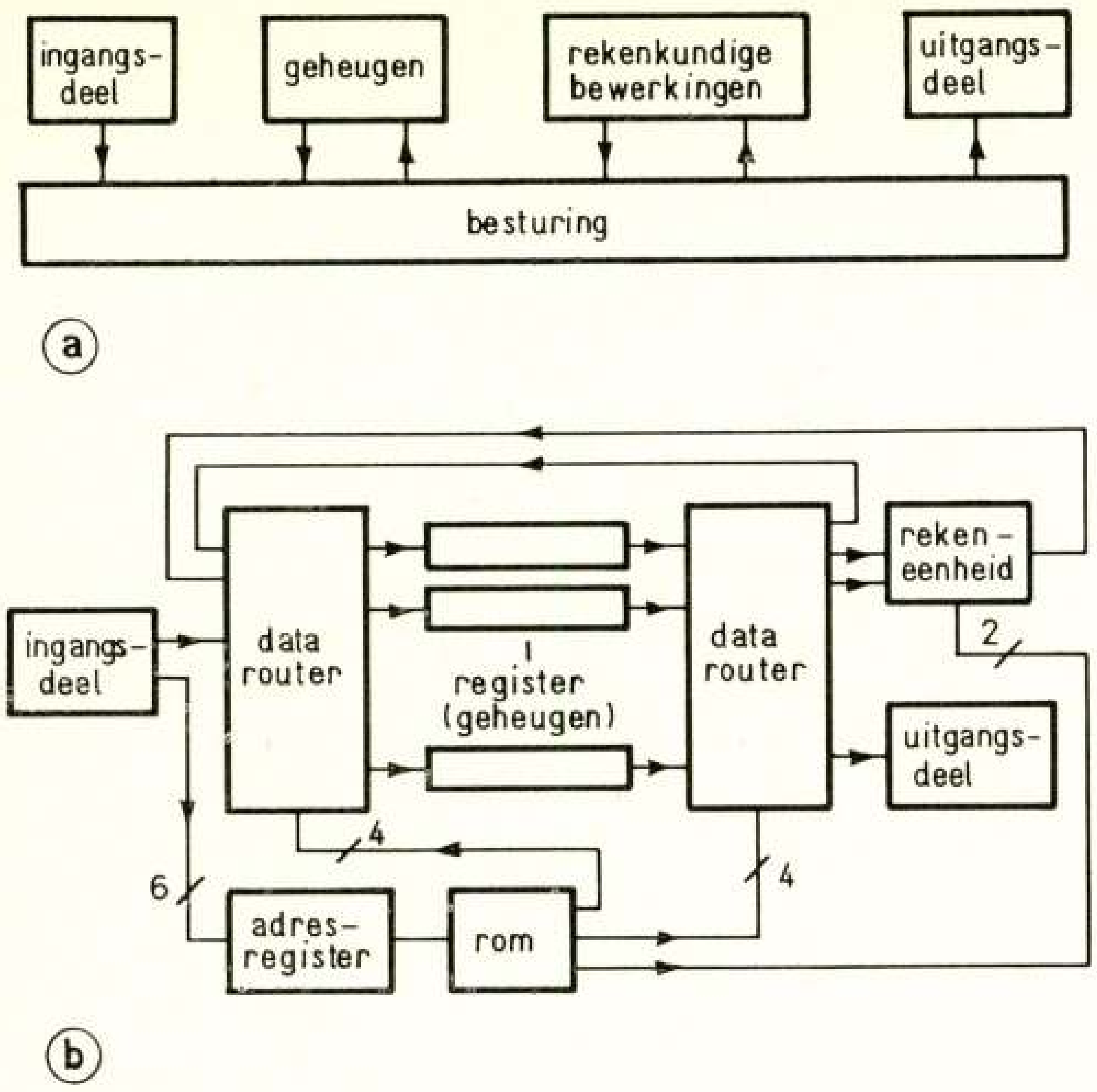


Fig. 1. Opzet van een tafelrekenmachine.
a. Fundamentele opzet, sterk vereenvoudigd;
b. Uitwerking met 'data routers' en 'read-only memory' (ROM.).
De mogelijkheden van een machine worden bepaald door de inhouden van de 'data routers' en 'read-only memories'. Met betrekkelijk geringe kosten kan men, door wijzigingen in data-routers en read-only memories komen tot de opzet van de gewenste variant.

3.2. *Analogie read-only memory en logische schakelingen*

Dat men met een 'read-only memory' hetzelfde kan bereiken als met de gebruikelijke logische schakelingen kan uit het volgende blijken: wij kunnen de adresingangen van het 'read-only memory' vergelijken met de ingangen van logische schakelingen. Voor iedere uitgang kan men nu de logische formule afleiden door voor iedere 1 in de tabel de bijbehorende *ingangs*signalen als produkt op te schrijven (EN-functie) en deze produkttermen te sommeren (OF-functie). Anders gezegd: het 'read-only memory' maakt in het selectie-deel eerst alle EN-functies die er met de ingangsvariabelen en hun inverse waarden mogelijk zijn; met de in de schakeling opgenomen matrix kiest men dan, welke termen men voor de betreffende uitgang in een OF-functie wil verenigen. Dit lijkt op het eerste gezicht niet erg efficiënt, maar het is het wel omdat de lay-out van het 'read-only memory' zo regelmatig en daardoor zo efficiënt is.

3.3. *Besparing data router ten opzichte van read-only memory*

Zoals gezegd zijn de 'data router' en het 'read-only memory' sterk verwant. De data router is echter voor zijn plaats in de rekenmachine economischer. Het door ons ontwikkelde type heeft 5 ingangen, 5 uitgangen en 4 adresingangen en vergt derhalve $5 \times 5 \times 2^4 = 400$ bits. Hetzelfde zou men met een 'read-only memory' kunnen bereiken, dat dan echter 9 adresingangen zou bezitten en 5 uitgangen en daarmee $2^9 \times 5 = 2560$ bits groot zou zijn. De 'data router' is dus duidelijk in het voordeel.

Men kan zich nu afvragen waardoor dit voordeel is verkregen. Het wordt veroorzaakt door twee beperkingen inherent aan de

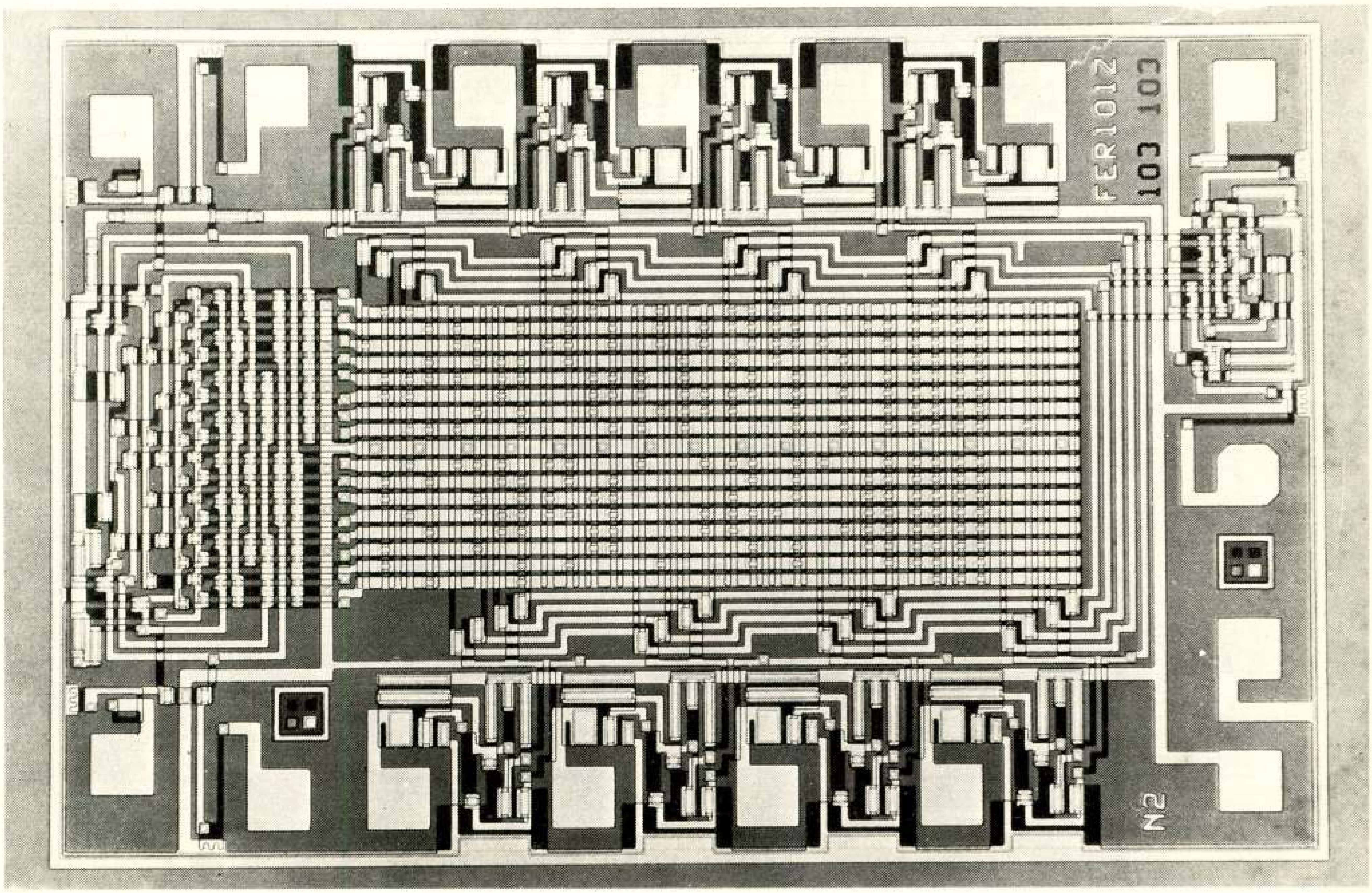


Fig. 2. Het kristal van een read-only memory van 64 woorden van 8 bits, totaal 512 bits, type FER101, afmetingen 1,47 bij 2,15 mm. Let op de regelmatige en daardoor efficiënte structuur met aluminiumlijnen loodrecht op diffusiebanen. Een 'data router' heeft een analoge opzet.

'data router'. Het 'read-only memory' kan *alle* logische functies leveren die er met de ingangsvariabelen mogelijk zijn, de 'data router' echter niet. Die kan van de data-ingangen niet de inverse signalen afleiden, waardoor er geen EN-functies verkregen kunnen worden. Een OF-functie is wel mogelijk.

4. Hoe op een kristal?

4.1. *Oude manier van maskers maken*

De gebruikelijke methode van maskers maken, waarbij voor alle 4 of 5 maskers, met behulp van een coördinatentafel de gewenste omtrekken in een dubbellaags materiaal worden ingesneden, waarna de bovenste, gekleurde laag met de hand wordt afgepeld, wordt bekend verondersteld.

Als de mate van integratie toeneemt krijgt deze methode enkele bezwaren:
- bij een kleine vergissing is het hele werk bedorven;
- bevat de schakeling vele malen dezelfde onderdelen dan moet toch alles afzonderlijk getekend en gesneden worden.

4.2. *Maskergenerator en CIRCUITMASK*

Bij de nieuwe methode van maskervervaardiging wordt gebruik gemaakt van een maskergenerator en het programma CIRCUITMASK. De maskergenerator kan fotografisch rechthoeken van de gewenste afmetingen op de gewenste plaatsen afbeelden. De generator wordt gestuurd door een ponsband; dit heeft het voordeel dat men voor een fout slechts de ponsband hoeft te corrigeren en niet alles behoeft over te doen. Stripfouten komen uiteraard niet meer voor daar de machine fotografisch werkt.

CIRCUITMASK is een computerprogramma voor het maken van de ponsband, die de maskergenerator bestuurt. Dit programma werkt met *standaard-onderdelen* waarvan de gegevens voor alle maskers in het geheugen van de computer aanwezig zijn. Met één code kan men zodoende het hele onderdeel oproepen en voor alle maskers tegelijk op de gewenste plaats aanbrengen. Uit deze standaard-onderdelen zijn weer *standaard-schakelingen* opgebouwd die eveneens in het geheugen van de computer zijn opgeslagen en op dezelfde manier als de standaard-onderdelen gebruikt kunnen worden.

Komt een onderdeel of schakeling *een aantal malen* voor, zoals dat in MOS-schakelingen zo vaak gebeurt (fig. 3 en fig. 4), dan behoeft men slechts de steek en het aantal op te geven. Het spreekt vanzelf dat dit een enorme besparing aan tekenwerk oplevert en dat er aanmerkelijk minder kans op fouten bestaat.

4.3. *Werkwijze maskers read-only memory en data router*

Een afnemer die een 'read-only memory' of een 'data router' wil bestellen specificeert de gewenste inhoud door het invullen

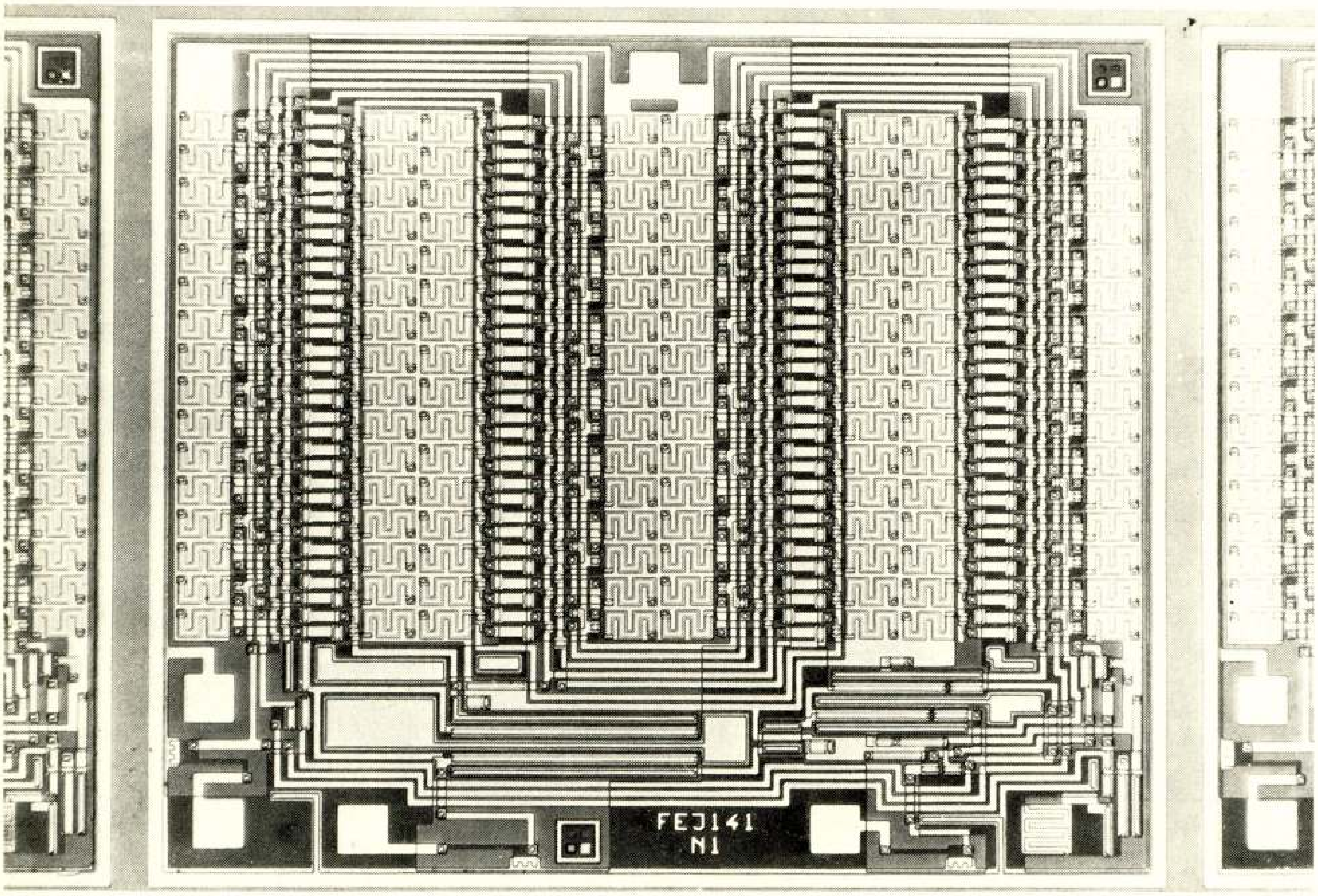


Fig. 3. Kristal van het 64-bits schuifregister, heen en weer schuivend, type FEJ141, afmetingen 1,9 bij 2,2 mm. Voor dergelijke typen, waarin éénzelfde grondschakeling vele malen herhaald wordt, betekenen de maskergenerator en het programma CIRCUITMASK een enorme besparing aan werk en een sterk verminderde kans op fouten.

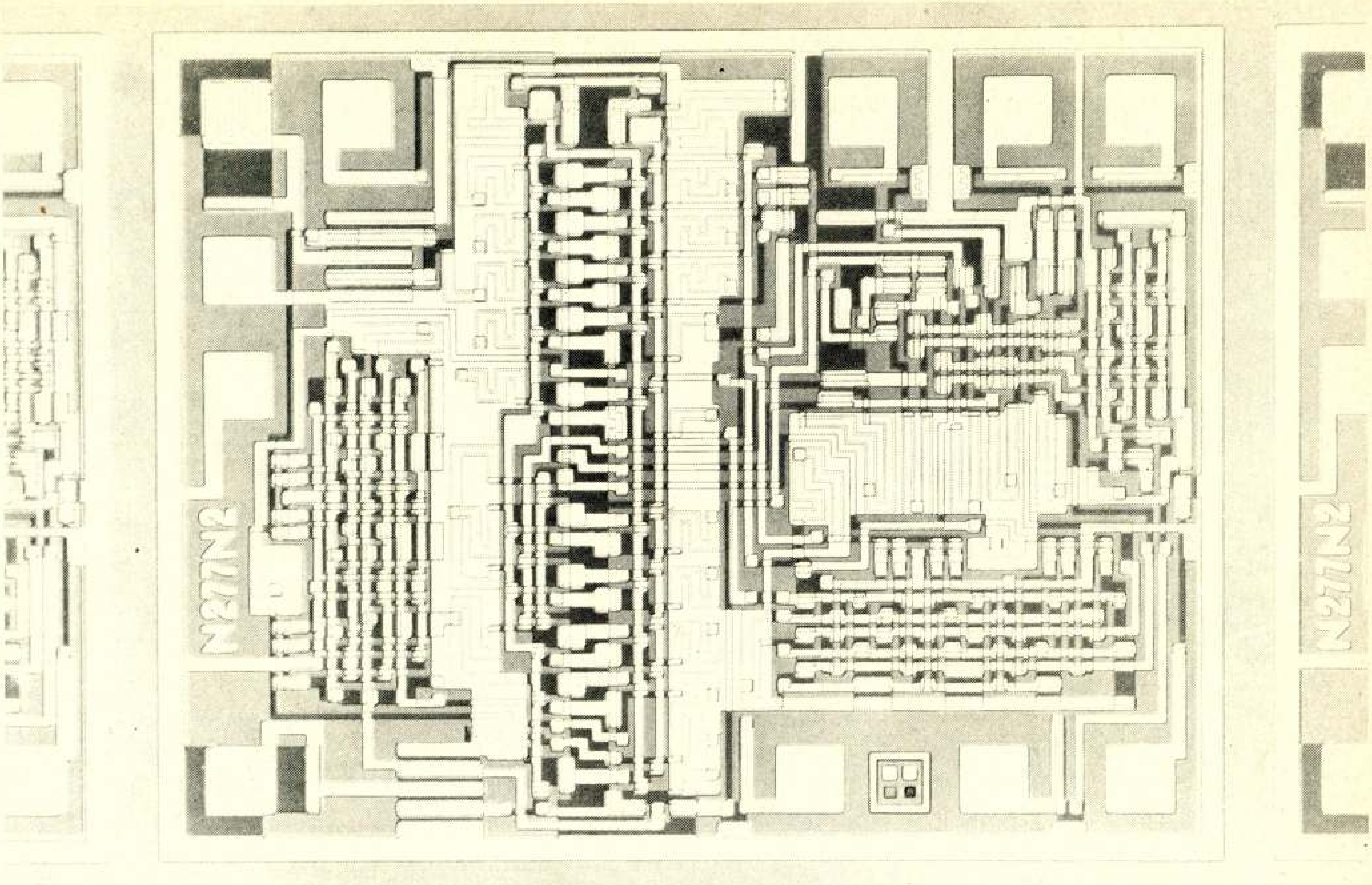


Fig. 4. Kristal van de 'serial decimal arithmetic unit', type FEJ241, afmetingen 1,33 bij 1,67 mm. In dit type komen twee 'binary full adders' voor, die niet uit poorten zijn samengesteld, maar als een klein 'read-only memory' zijn verwezenlijkt; zij bevinden zich links en rechts onder en zijn te herkennen aan hun regelmatige structuur.

van een tabel. Na ontvangst vullen wij eerst het typenummer in, dat deze schakeling verder zal karakteriseren, en nemen dan de inhoud op een ponsband over. De ponsband wordt in de computer gevoerd, die hem controleert op fouten.

Daarna combineert hij de inhoud met de gegevens van het vaste deel van de lay-out, die in het geheugen aanwezig zijn en produceert vervolgens de ponsband voor de maskergenerator.

Via maskers en diffusie wordt zo het gewenste produkt gemaakt, dat dan nog getest moet worden. Dezelfde ponsband die de computer programmeerde wordt hiertoe in de tester ingevoerd, waarin hij wordt gecombineerd met het algemene testprogramma dat in het geheugen van de tester aanwezig is.

Op deze wijze wordt, met een minimum aan werk en dus een minimum aan kosten, bij minimale kans op fouten een nieuw type geïntegreerde schakeling geproduceerd. Het is aldus thans mogelijk een grote verscheidenheid van rekenmachines samen te stellen uit telkens dezelfde standaard-schakelingen (zoals schuifregisters) aangevuld met 'data routers' en 'read-only memories', waarbij de verscheidenheid geheel wordt opgevangen in deze beide laatste typen.

Korte technische berichten

Reorganisatie INTELSAT

Op 21 mei jl. werd de slotzitting gehouden van de Plenipotentiaire Conferentie voor de definitieve regeling van het Internationale Telecommunicatie Satellieten Consortium (INTELSAT), waaraan door delegaties van 78 van de 79 lidstaten van INTELSAT werd deelgenomen en waarin de eindtekst van een nieuwe overeenkomst werd aanvaard.

Dit nieuwe verdrag wordt van kracht, wanneer het is ondertekend door tweederde van de lidstaten, die bovendien samen voor tweederde participeren in het bedrijfskapitaal van INTELSAT. Van 20 augustus 1971 af ligt het verdrag open voor ondertekening.

Door dit verdrag wordt de structuur van de organisatie ingrijpend veranderd. Tot nu toe bestaan er twee organen, een Interimcomité als beleidsinstantie en een beheersinstantie, belichaamd in de Amerikaanse maatschappij COMSAT.

Het nieuwe verdrag voorziet in vier organen op onderscheiden niveaus:

– een *Assemblee van Lidstaten*, die de inspraak van de regeringen in de organisatie verzekert;

– een *Algemene Vergadering* van lid-deelnemers, welke met name omtrent exploitatieve aangelegenheden adviserende bevoegdheid bezit; de lid-deelnemers exploiteren het telecommunicatienet;

– een *Raad van Bestuur*, bestaande uit 20 tot 25 leden, op basis

van het investeringsaandeel, met de verantwoordelijkheid om het wereldomspannende, internationale stelsel van telecommunicatiesatellieten voort te zetten en verder uit te breiden;
– een *Uitvoerend Orgaan*, onder leiding van een directeur-generaal als wettelijke vertegenwoordiger van INTELSAT.

Als overgangsmaatregel zal, krachtens een contract met de Raad van Bestuur, gedurende zes jaar na het van kracht worden van de nieuwe overeenkomst het management in handen van COMSAT blijven. Voor deze periode zal voor de administratieve werkzaamheden een secretaris-generaal worden benoemd.

Ir. F. Maarleveld.

Ingebruikneming van het nieuwe ITT research-laboratorium bij Parijs

In een der Parijse voorsteden is in de industriewijk Vélizy, tegenover het Foret de Meudon, een nieuw laboratorium in gebruik genomen voor het Research Centrum van de International Telephone and Telegraph Corporation (ITT). Tot nu toe was dit Centrum in het hart van Parijs gevestigd. In het oude Centrum werd veel pionierswerk verricht op het gebied van de telecommunicatie, luchtvaart- en ruimtenavigatie, dataverwerking, radar, lasertechniek en van dunne-film geheugens.

Het nieuwe laboratorium heeft een nuttig vloeroppervlak van bijna 14 000 m^2 en is volledig met air-conditioning uitgerust. De personeelsbezetting van wetenschappelijke medewerkers tot lagere technici omvat ongeveer 400 personen.

ITT.

Televisieprogramma's naar eigen keuze

In Groot-Brittannië is onlangs het *Electronic Video Recording* systeem geïntroduceerd, dat het kijkers mogelijk maakt programma's van hun eigen keuze op hun eigen televisie-ontvangers te zien.

De programma's zijn vastgelegd op speciale 8.77 mm films die worden geleverd in 17.5 cm cassettes; zij kunnen door een op het TV-toestel aangesloten 'telespeler' ter grootte van een bandopnemingsapparaat worden afgespeeld.

De cassettes worden in Engeland op de markt gebracht door EVR Partnership. De telespelers worden vervaardigd door Rank Bush Murphy Ltd.

Vele Britse programma-eigenaren hebben bij EVR-Partnership orders geplaatst voor de transcriptie van belangrijk onderwijsmateriaal. Ook zijn overeenkomsten afgesloten met vooraanstaande programma-organisaties in Frankrijk, Duitsland, Italië, Scandinavië en Zwitserland. EVR-Partnership verwacht te zijner tijd een miljoen cassettes per jaar te kunnen produceren. Er zou thans reeds een bibliotheek met meer dan 300 programma's opgebouwd zijn.

Men is van mening dat het systeem vooral enorme mogelijkheden heeft op het gebied van het onderwijs.

London Press Service.

MOS-technieken

De aflevering 7-8-9 uit de jaargang 1970 van Philips Technisch Tijdschrift werd geheel aan MOS-transistors en -schakelingen gewijd. Een aantal belangwekkende aspecten betreffende de technologie en werking en de opzet van enige analoge en digitale schakelingen komen in een keur van artikelen aan de orde. Na kennisneming is de lezer een aantal zeer waardevolle inzichten rijker geworden.

Leergang Elektronische Meetapparatuur

Op *27, 28 en 29 september 1971* organiseert de Afdeling voor Elektrotechniek van het Koninklijk Instituut van Ingenieurs in samenwerking met de Afdeling der Elektrotechniek van de Technische Hogeschool te Delft, een leergang over moderne ontwikkelingen bij de elektronische meetapparatuur. In een vijftiental voordrachten zullen onderwerpen uit een aantal gebieden worden behandeld.

De leergang wordt gehouden in het gebouw voor Elektrotechniek te Delft.

De Secretaris van de Afdeling voor Elektrotechniek,
ir. H. J. Roosdorp.

Uit het NERG

Administratie van het NERG: Postbus 39, Leidschendam.
Giro 94746 t.n.v. penningmeester NERG, Leidschendam.
Secretariaat van de Examencommissie-NERG: von Geusaustraat 151, Voorburg.

Prof. dr. ir. A. A. Th. M. van Trier lid van het Bestuur van TNO*)

Op voordracht van de Minister van Onderwijs en Wetenschappen heeft de Koningin prof. dr. ir. A. A. Th. M. van Trier benoemd tot lid van het Bestuur van de Centrale Organisatie TNO. Vanaf 1 januari 1972 zal prof. Van Trier, gezamenlijk met de huidige ondervoorzitter, ir. E. F. Boon, leiding gaan geven aan TNO.

Prof. Van Trier, sinds 1 september 1968 Rector Magnificus van de T.H. Eindhoven, zal tot eind 1971 zijn rectoraat blijven vervullen. Aan zijn benoeming indertijd tot Rector Magnificus en aan de vele activiteiten die prof. Van Trier ontplooit, werd o.a. in 'De Ingenieur' 1968, nr. 16, blz. ET 60, aandacht geschonken.

In verband met drukke werkzaamheden trad prof. Van Trier in april 1971 uit het Bestuur van het NERG.

Ledenmutaties

Voorgestelde leden
Ir. G. K. F. van der Woud, Reigerlaan 20, Boskoop.

Nieuwe leden
Ir. P. Groenveld, Pisanostraat 444, Eindhoven.
Ir. C. van Holten, Bergsingel 30 B, Rotterdam.
Ir. E. H. Nordholt, Arthur van Schendelplein 163, Delft.
Ir. A. Willemsen, Dillenburgsingel 3, Leidschendam.

Nieuwe adressen van leden
Tj. Douma, B 116, Ezumazijl onder Anjum (Fr.).
Ir. F. P. van Enk, Lange Nieuwstraat 23 B, Schiedam.
Ir. D. W. Rollema, Van der Marckstraat 5, Leiderdorp.

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*) Zie ook 'De Ingenieur' 1971, nr. 17, blz. A 292.